

### Features

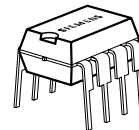
- Output voltage tolerance  $\leq \pm 2\%$
- Very low current consumption
- Early warning
- Reset output low down to  $V_Q = 1\text{ V}$
- Overtemperature protection
- Reverse polarity proof
- Settable reset threshold
- Very low drop voltage
- Wide temperature range
- Integrated pull up resistor at logic outputs

Type	Ordering Code	Package
TLE 4269 A	Q67000-A9190	P-DIP-8-4
TLE 4269 G	Q67006-A9173	P-DSO-8-1 (SMD)
▼ TLE 4269 GM	Q67006-A9288	P-DSO-14-4 (SMD)
TLE 4269 GL	Q67006-A9192	P-DSO-20-6 (SMD)

▼ New type

### Functional Description

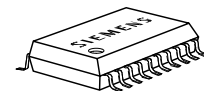
This device is a voltage regulator with a fixed 5-V output, e.g. in a P-DSO-8-1 package. The maximum operating voltage is 45 V. The output is able to drive a 150 mA load. It is short circuit protected and the thermal shutdown switches the output off if the junction temperature is in excess of 150 °C. A reset signal is generated for an output voltage of  $V_Q < 4.6\text{ V}$ . The reset threshold voltage can be decreased by external connection of a voltage divider. The reset delay time can be set by an external capacitor. Reset and sense output have integrated pull up resistors. If the integrated resistors are not desired **TLE 4279** can be used. It is also possible to supervise the input voltage by using an integrated comparator to give a low voltage warning.



**P-DIP-8-4**



**P-DSO-8-1**

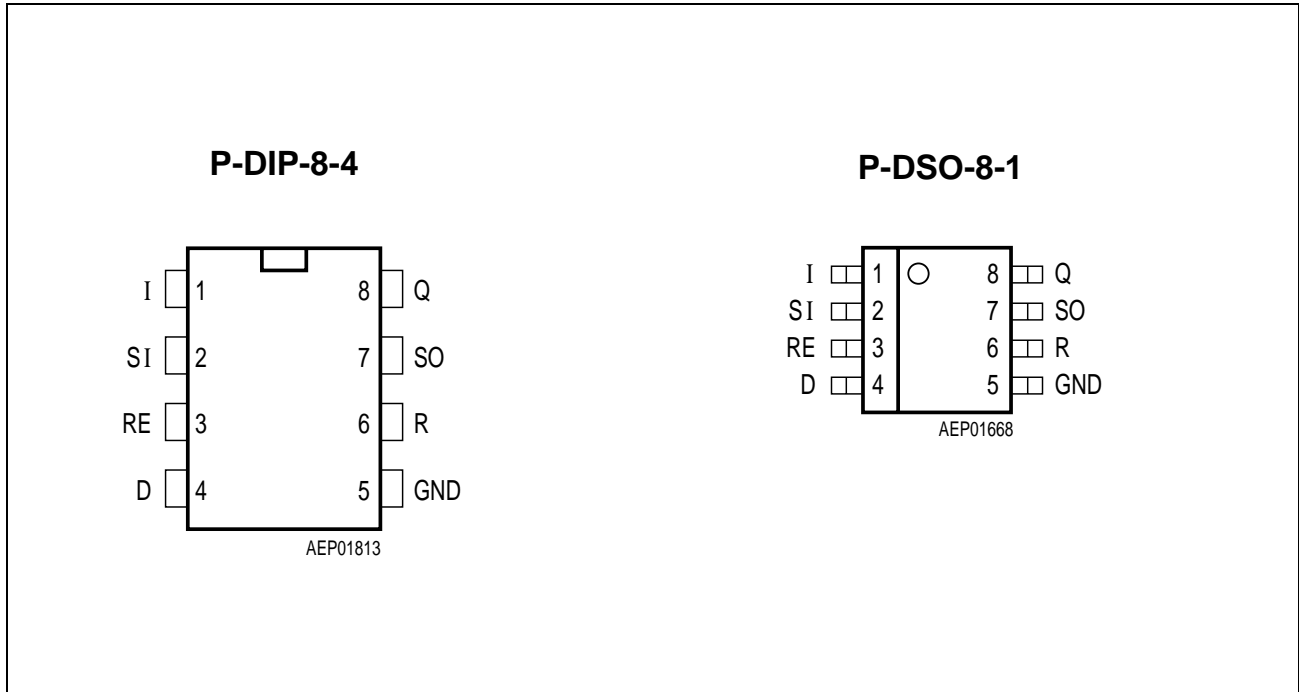


**P-DSO-20-6**



**P-DSO-14-4**

**Pin Configuration**  
(top view)

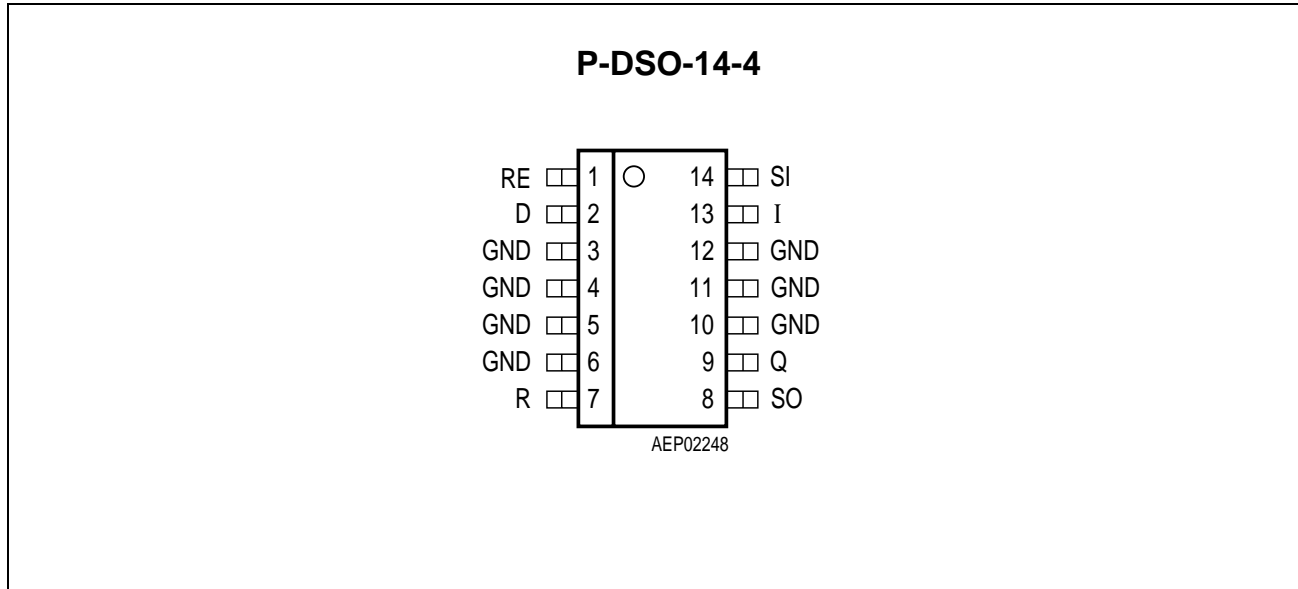


**Pin Definitions and Functions (TLE 4269 A and TLE 4269 G)**

Pin No.	Symbol	Function
1	I	<b>Input</b> ; block directly to GND on the IC with a ceramic capacitor.
2	SI	<b>Sense Input</b> ; if not needed connect to Q.
3	RE	<b>Reset Threshold</b> ; if not needed connect to ground.
4	D	<b>Reset Delay</b> ; to select delay time, connect to GND via external capacitor.
5	GND	<b>Ground</b>
6	R	<b>Reset Output</b> ; the open-collector output is internally linked to Q via a 20 kΩ pull-up resistor.
7	SO	<b>Sense Output</b> ; the open-collector output is internally linked to the output via a 20 kΩ pull-up resistor.
8	Q	<b>5-V Output</b> ; connect to GND with a 10 μF capacitor, ESR < 10 Ω.

**Pin Configuration**

(top view)

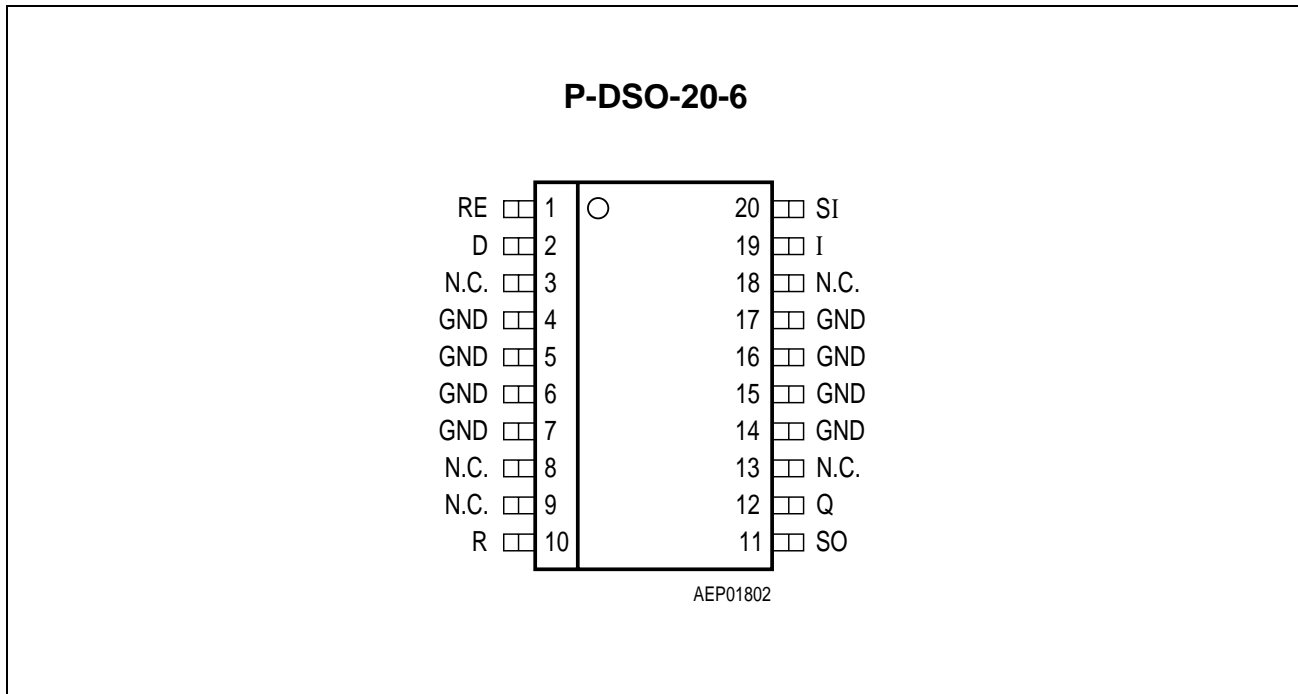


**Pin Definitions and Functions (TLE 4269 GM)**

Pin No.	Symbol	Function
1	RE	<b>Reset Threshold</b> ; if not needed connect to GND.
2	D	<b>Reset Delay</b> ; connect to GND via external delay capacitor for setting delay time.
3, 4, 5, 6	GND	<b>Ground</b>
7	R	<b>Reset Output</b> ; open-collector output, internally connected to Q via a pull-up resistor of 20 kΩ.
8	SO	<b>Sense Output</b> ; open-collector output, internally connected to Q via a 20 kΩ pull-up resistor.
9	Q	<b>5-V Output</b> ; connect to GND with a 10 μF capacitor, ESR < 10 Ω.
10, 11, 12	GND	<b>Ground</b>
13	I	<b>Input</b> ; block to GND directly at the IC by a ceramic capacitor.
14	SI	<b>Sense Input</b> ; if not needed connect to Q.

**Pin Configuration**

(top view)



**Pin Definitions and Functions (TLE 4269 GL)**

Pin No.	Symbol	Function
1	RE	<b>Reset Threshold;</b> if not needed connect to GND.
2	D	<b>Reset Delay;</b> to select delay time connect to GND via external capacitor.
4-7, 14-17	GND	<b>Ground</b>
10	R	<b>Reset Output;</b> the open-collector output is internally linked to Q via 20 kΩ pull-up resistor.
11	SO	<b>Sense Output;</b> the open-collector output is internally linked to Q via 20 kΩ pull-up resistor.
12	Q	<b>Output;</b> connect to GND with a 10 μF capacitor, ESR < 10 Ω.
19	I	<b>Input;</b> block directly to GND at the IC by a ceramic capacitor.
20	SI	<b>Sense Input;</b> if not needed connect to Q.

## Circuit Description

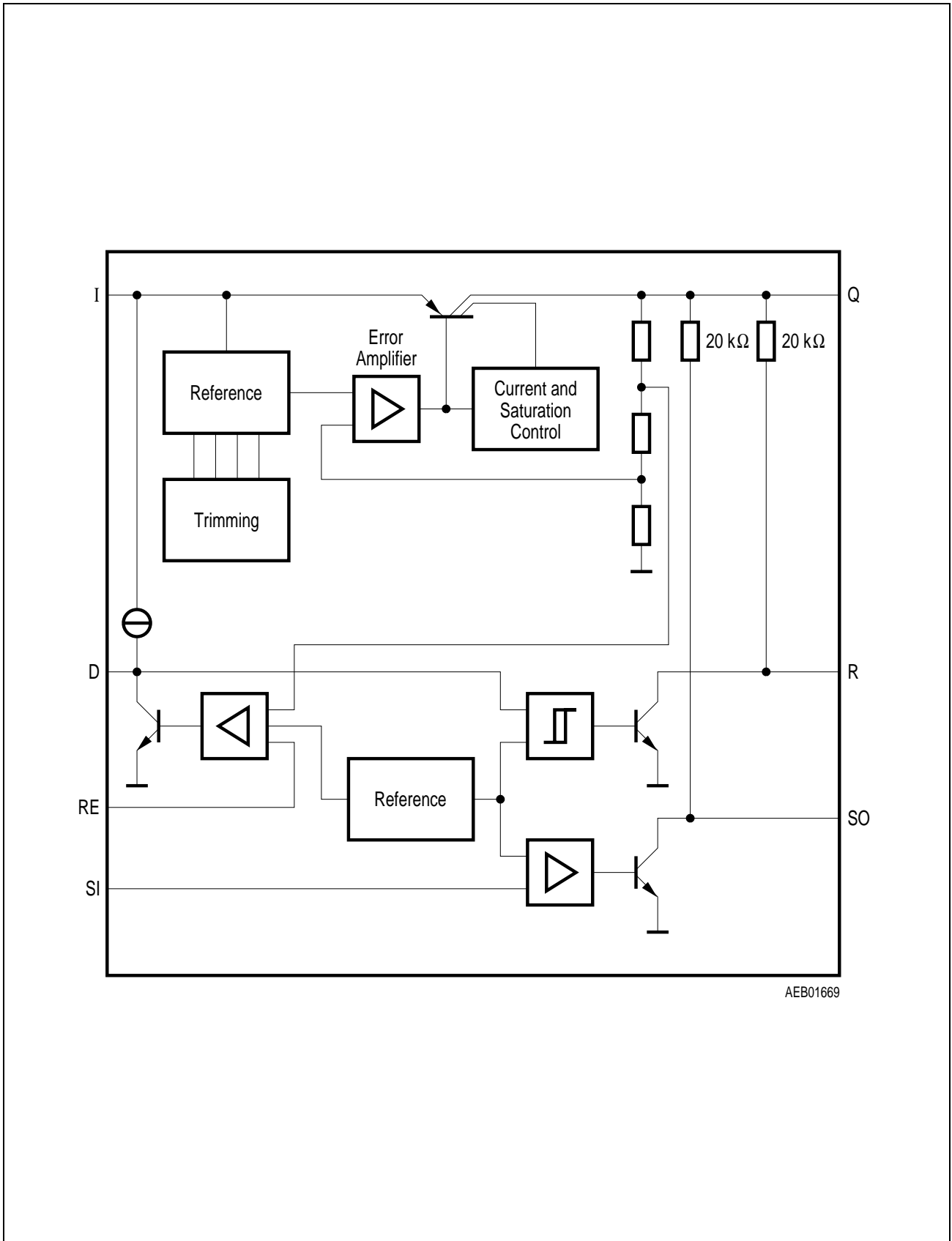
The control amplifier compares a reference voltage, made highly accurate by resistance balancing, with a voltage proportional to the output voltage and drives the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element.

In the reset generator block a comparator compares a reference voltage independent of the input voltage with the scaled-down output voltage. If the output voltage reaches 4.6 V the reset delay capacitor is discharged and the reset output is set to low. This low is guaranteed down to an output voltage of 1 V. As the output voltage increases again, from 4.6 V onward the reset delay capacitor is charged with constant current. When the capacitor voltage reaches the upper switching threshold  $V_{dT}$ , the reset returns to high. By choosing the value of this capacitor, the reset delay time can be selected over a wide range. With the reset threshold input RE it is possible to lower the reset threshold  $V_{rt}$ . If pin RE is connected to pin Q via a voltage divider, for example, the reset condition is reached when this voltage is decreased below the switching threshold  $V_{re}$  of 1.35 V.

Another comparator compares the signal of the pin SI, normally fed by a voltage divider from the input voltage, with the reference and gives an early warning on the pin SO. It is also possible to supervise an other voltage e.g. of a second regulator, or to build a watchdog circuit with few external components.

## Application Description

The input capacitor  $C_i$  is necessary for compensating line influences. Using a resistor of approx. 1  $\Omega$  in series with  $C_i$ , the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor  $C_o$  is necessary for the stability of the regulating circuit. Stability is guaranteed at values  $\geq 10 \mu\text{F}$  and an ESR  $\leq 10 \Omega$  within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.



Block Diagram

**Absolute Maximum Ratings**

$T_j = -40$  to  $150$  °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		

**Input**

Input voltage	$V_I$	- 40	45	V	–
Input current	$I_I$	–	–	–	internal limited

**Sense Input**

Input voltage	$V_{SI}$	- 0.3	45	V	–
Input current	$I_{SI}$	1	1	mA	–

**Reset Threshold**

Voltage	$V_{RE}$	- 0.3	7	V	–
Current	$I_{RE}$	- 10	10	mA	–

**Reset Delay**

Voltage	$V_D$	- 0.3	7	V	–
Current	$I_D$	–	–	–	internal limited

**Ground**

Current	$I_{GND}$	50	–	mA	–
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**Reset Output**

Voltage	$V_R$	- 0.3	7	V	–
Current	$I_R$	–	–	–	internal limited

**Absolute Maximum Ratings (cont'd)**

$T_j = -40$  to  $150$  °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		

**Sense Output**

Voltage	$V_{SO}$	- 0.3	7	V	-
Current	$I_{SO}$	-	-	-	internal limited

**5-V Output**

Output voltage	$V_Q$	- 0.3	7	V	-
Output current	$I_Q$	- 5	-	mA	-

**Temperature**

Junction temperature	$T_j$	-	150	°C	-
Storage temperature	$T_{Stg}$	- 50	150	°C	-

**Operating Range**

Input voltage	$V_I$	-	45	V	-
Junction temperature	$T_j$	- 40	150	°C	-

**Thermal Data**

Junction-ambient	$R_{thja}$	-	100 200 70 70	K/W K/W K/W K/W	P-DIP-8-4 P-DSO-8-1 P-DSO-14-4 P-DSO-20-6
	$R_{thjc}$	-	60 60 30 30	K/W K/W K/W K/W	P-DIP-8-4 P-DSO-8-1 P-DSO-14-4 P-DSO-20-6



**Characteristics**
 $V_1 = 13.5 \text{ V}; T_j = -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ 

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		min.	typ.	max.		
Output voltage	$V_Q$	4.90	5.00	5.10	V	$1 \text{ mA} \leq I_Q \leq 100 \text{ mA}$ $6 \text{ V} \leq V_1 \leq 16 \text{ V}$
Current limit	$I_Q$	150	200	500	mA	–
Current consumption; $I_q = I_1 - I_Q$	$I_q$	–	150	300	$\mu\text{A}$	$I_Q \leq 1 \text{ mA}, T_j < 85 \text{ }^\circ\text{C}$
Current consumption; $I_q = I_1 - I_Q$	$I_q$	–	250	700	$\mu\text{A}$	$I_Q = 10 \text{ mA}$
Current consumption; $I_q = I_1 - I_Q$	$I_q$	–	2	8	mA	$I_Q = 50 \text{ mA}$
Drop voltage	$V_{dr}$	–	0.25	0.5	V	$I_Q = 100 \text{ mA}^1)$
Load regulation	$\Delta V_Q$	–	10	30	mV	$I_Q = 5 \text{ mA to } 100 \text{ mA}$
Line regulation	$\Delta V_Q$	–	10	40	mV	$V_1 = 6 \text{ V to } 26 \text{ V}$ $I_Q = 1 \text{ mA}$

**Reset Generator**

Switching threshold	$V_{rt}$	4.50	4.60	4.80	V	–
Reset pull up	–	10	20	40	$\text{k}\Omega$	–
Reset low voltage	$V_R$	–	0.1	0.4	V	$R_{\text{intern}}$
Delay switching threshold	$V_{dt}$	1.4	1.8	2.2	V	–
Switching threshold	$V_{st}$	0.3	0.45	0.60	V	–
Reset delay low voltage	$V_D$	–		0.1	V	$V_Q < V_{RT}$
Charge current	$I_d$	3.0	6.5	9.5	$\mu\text{A}$	$V_D = 1 \text{ V}$

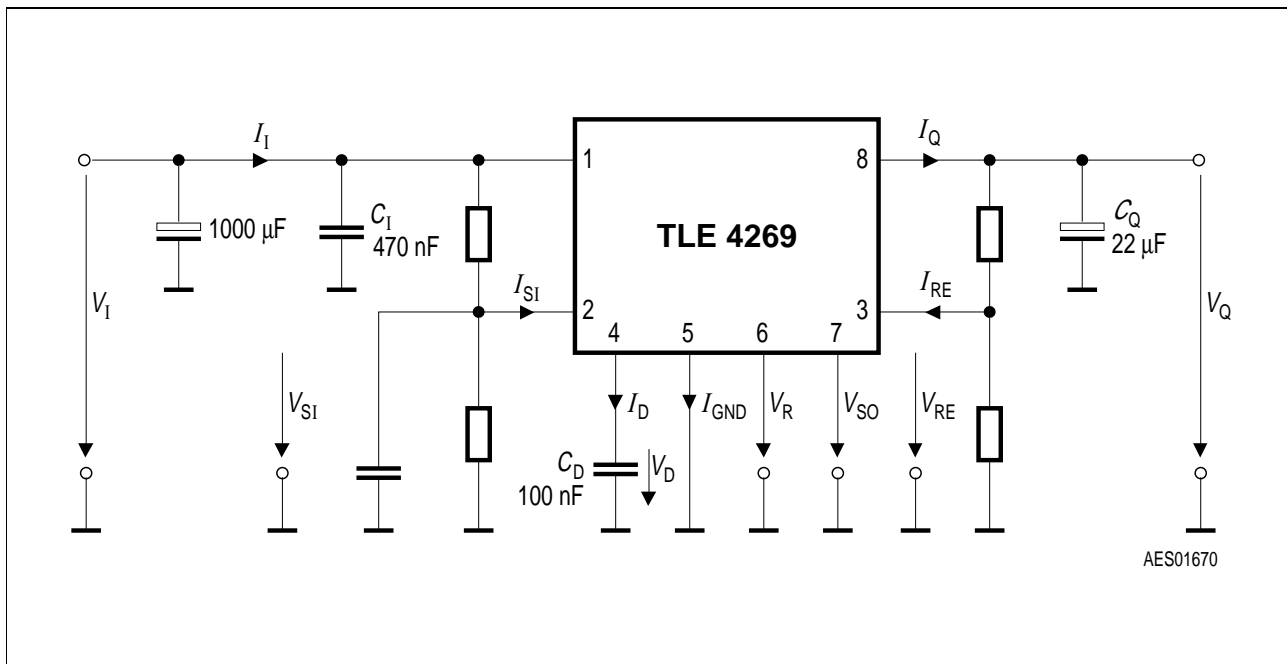
1) Drop voltage =  $V_1 - V_Q$  (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input.)

**Characteristics (cont'd)**
 $V_i = 13.5 \text{ V}; T_j = -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}$ 

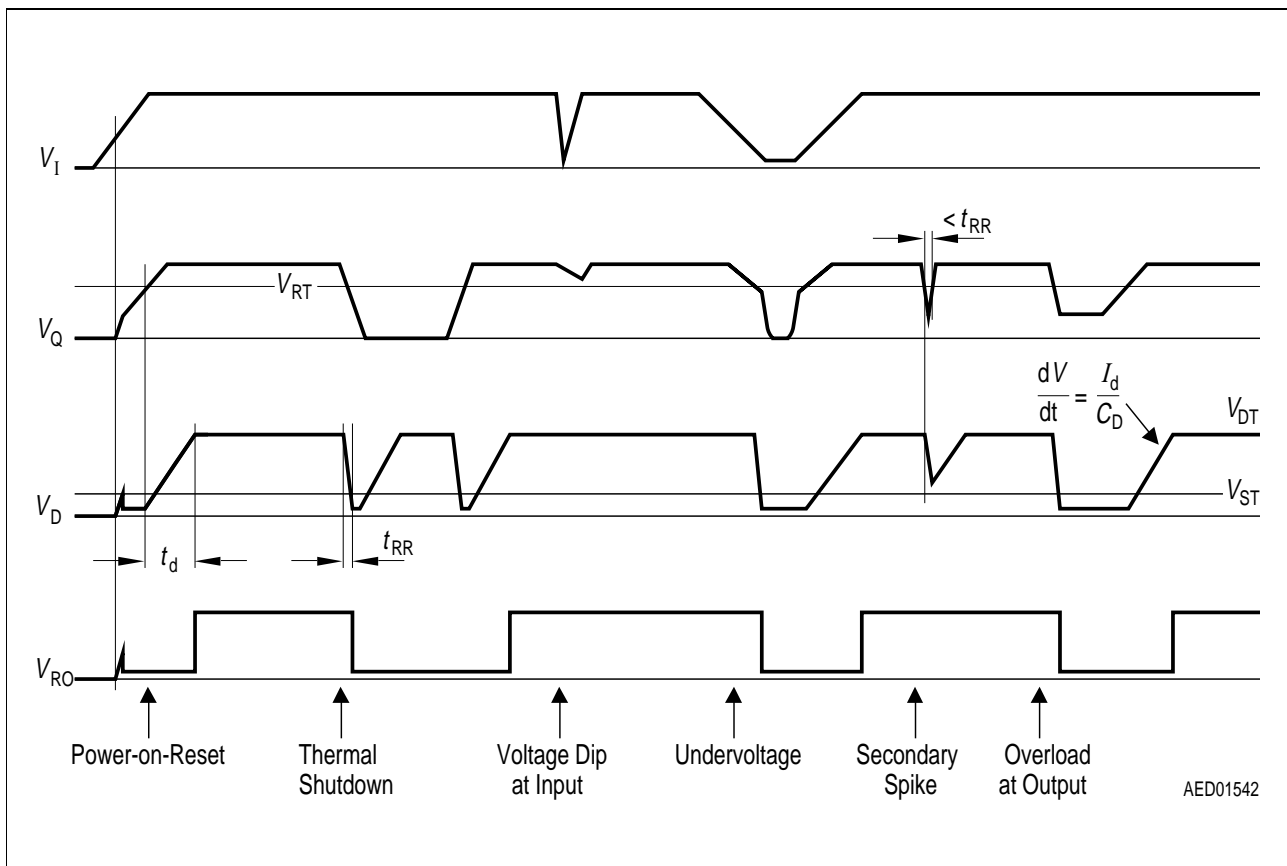
Parameter	Symbol	Limit Values			Unit	Measuring Condition
		min.	typ.	max.		
Delay time L → H	$t_d$	17	28	–	ms	$C_D = 100 \text{ nF}$
Delay time H → L	$t_t$	–	1	–	$\mu\text{s}$	$C_D = 100 \text{ nF}$
Switching voltage	$V_{re}$	1.26	1.35	1.44	V	$V_Q > 3.5 \text{ V}$

**Input Voltage Sense**

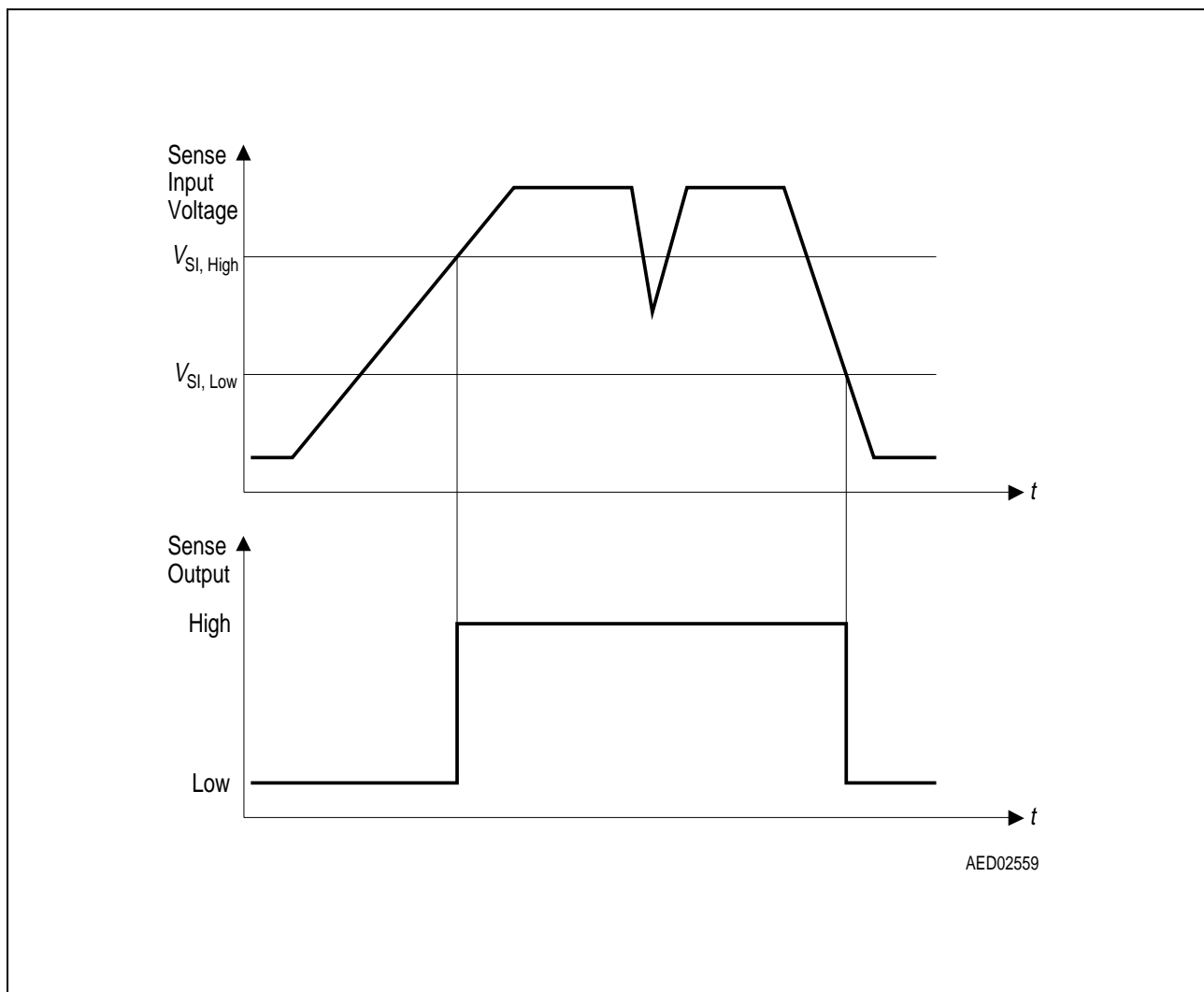
Sense threshold high	$V_{si, high}$	1.24	1.31	1.38	V	–
Sense threshold low	$V_{si, low}$	1.16	1.20	1.28	V	–
Sense output low voltage	$V_{SO, low}$	–	0.1	0.4	V	$V_{SI} < 1.20 \text{ V};$ $V_i > 3 \text{ V}$ $R_{intern}$
Sense pull up	–	10	20	40	$\text{k}\Omega$	–
Sense input current	$I_{SI}$	– 1	0.1	1	$\mu\text{A}$	–



Measuring Circuit (P-DIP-8-4/P-DSO-8-1)

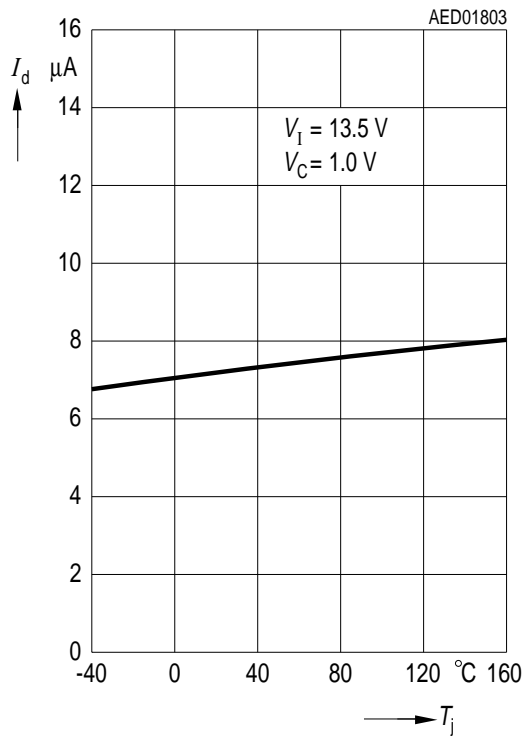


Reset Timing Diagram

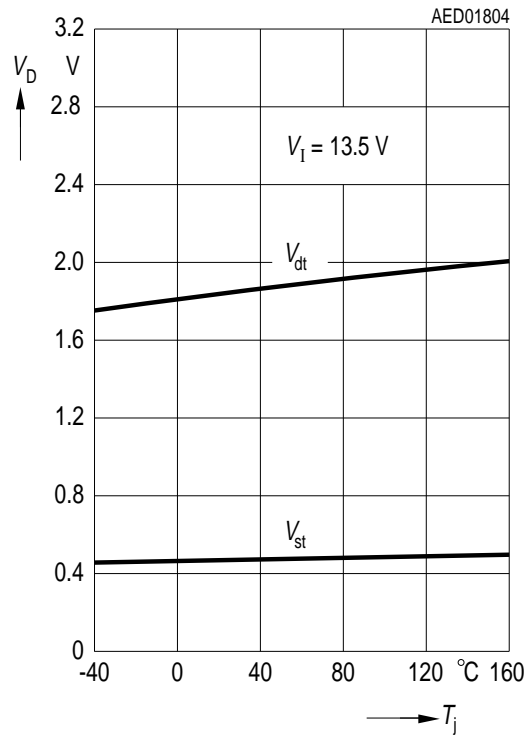


Sence Timing Diagram

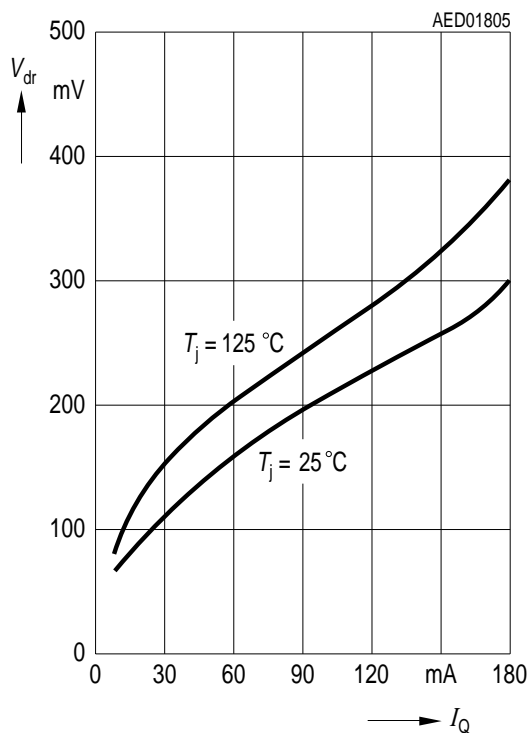
Charge Current  $I_d$  versus Temperature  $T_j$



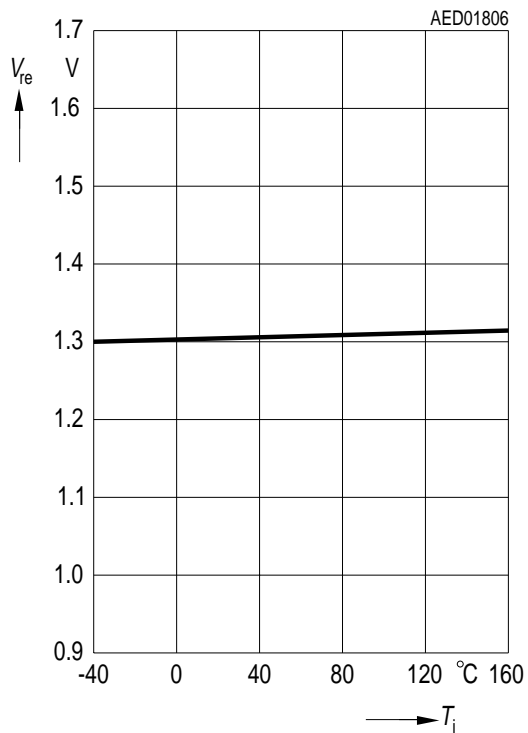
Switching Voltage  $V_{dt}$  and  $V_{st}$  versus Temperature  $T_j$



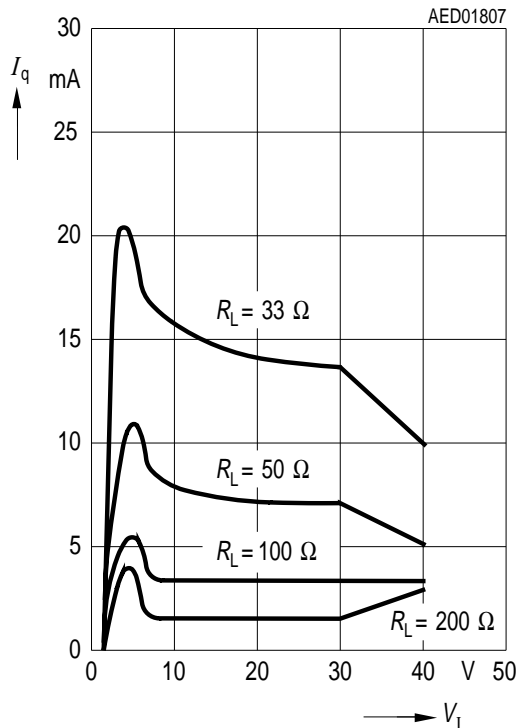
Drop Voltage  $V_{dr}$  versus Output Current  $I_Q$



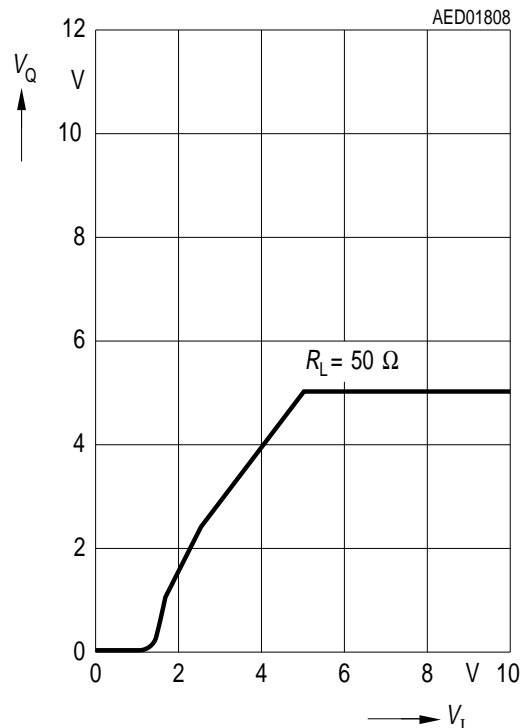
Reset Switching Threshold  $V_{re}$  versus Temperature  $T_j$



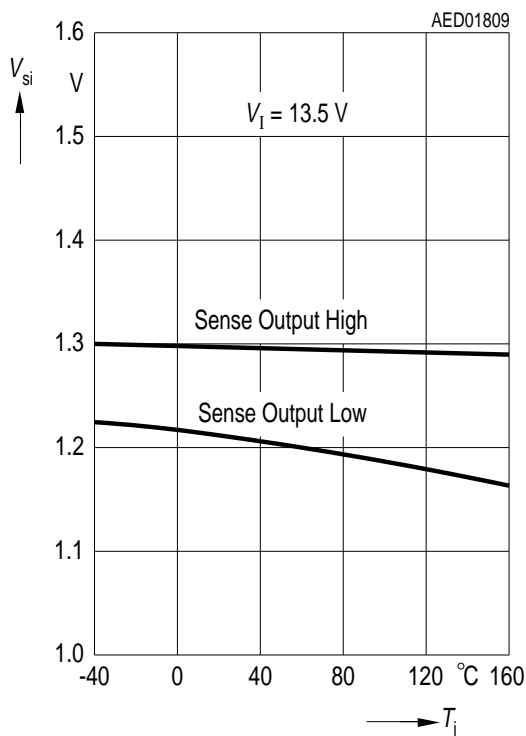
**Current Consumption  $I_Q$  versus Input Voltage  $V_I$**



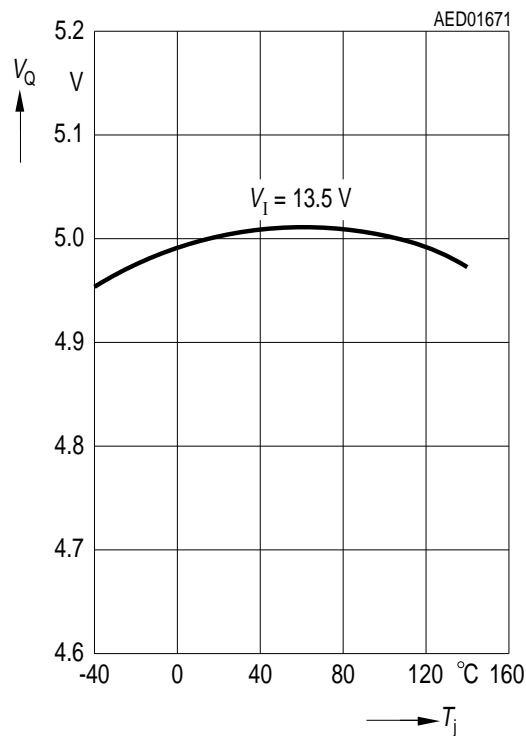
**Output Voltage  $V_Q$  versus Input Voltage  $V_I$**



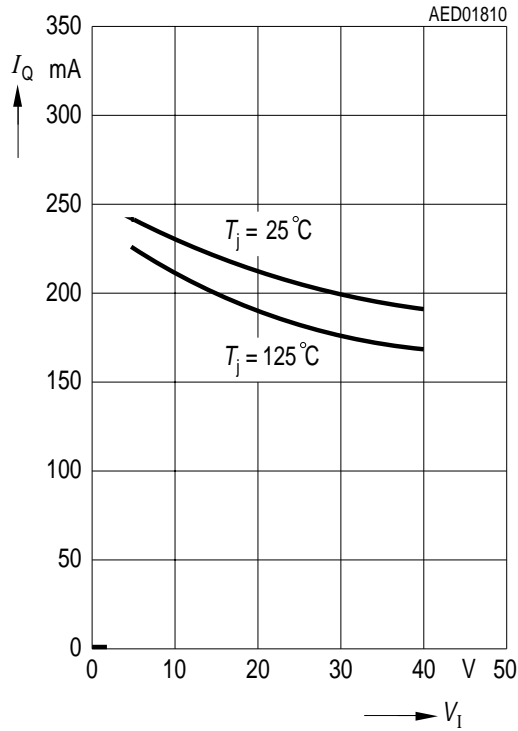
**Sense Threshold  $V_{si}$  versus Temperature  $T_j$**



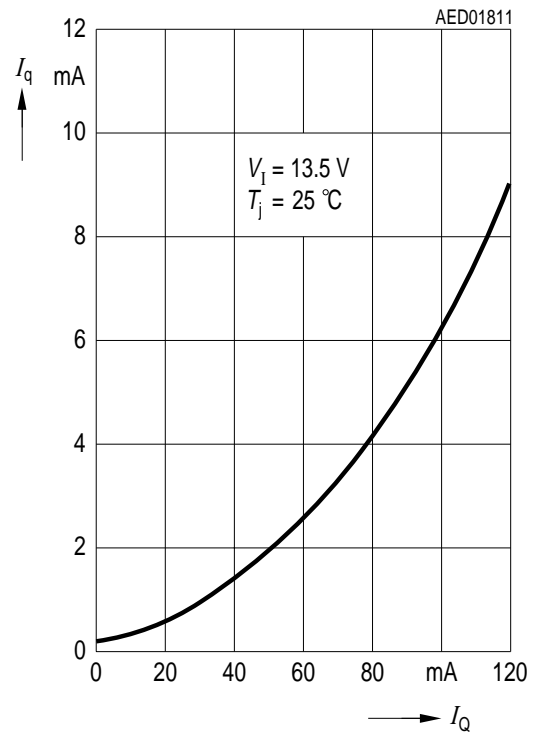
**Output Voltage  $V_Q$  versus Temperature  $T_j$**



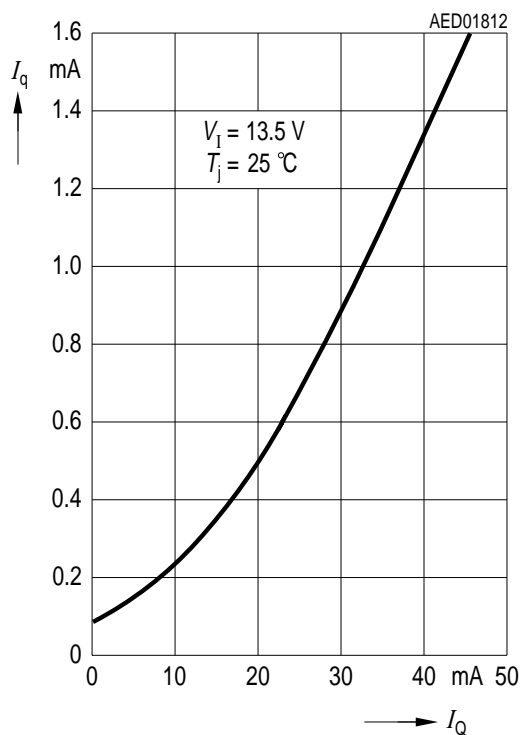
Output Current  $I_Q$  versus Input Voltage  $V_I$



Current Consumption  $I_q$  versus Output Current  $I_Q$

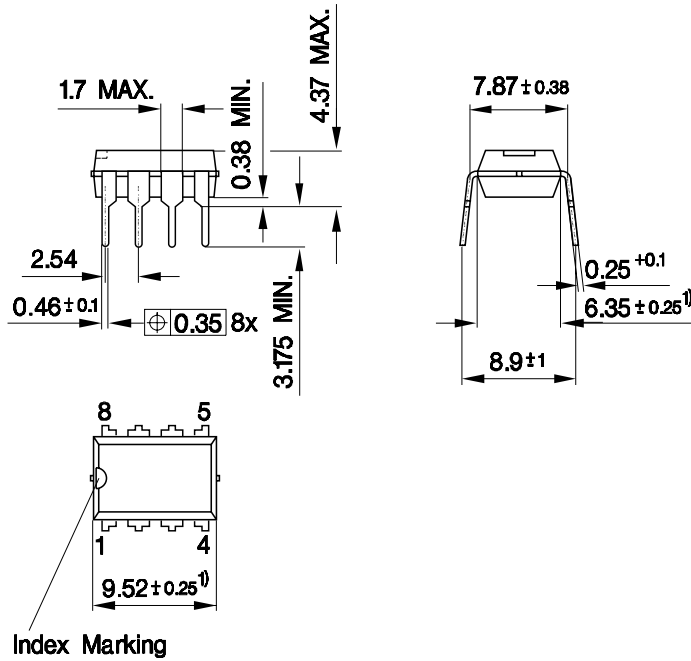


Current Consumption  $I_q$  versus Output Current  $I_Q$



Package Outlines

**P-DIP-8-4**  
(Plastic Dual In-line)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05583

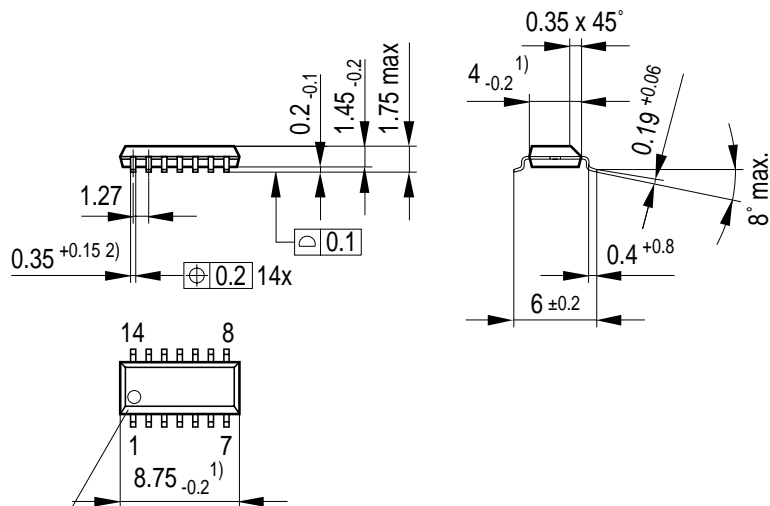
**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

Dimensions in mm



**P-DSO-14-4 (SMD)**  
(Plastic Dual Small Outline)



Index Marking

- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion of 0.05 max. per side

GPS05093

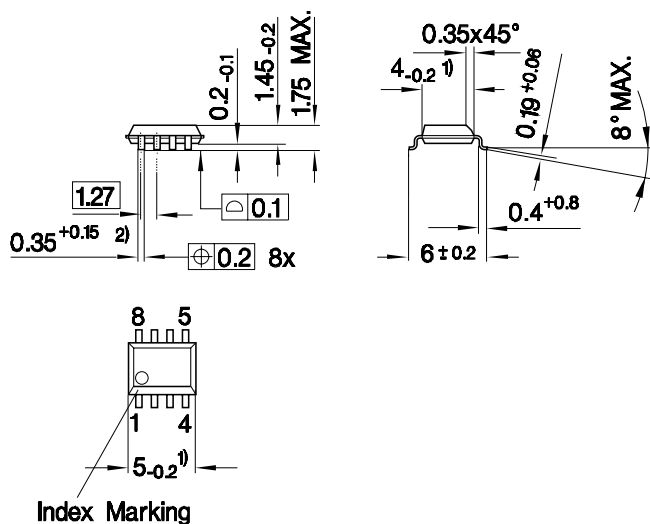
**Sorts of Packing**

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Dimensions in mm

SMD = Surface Mounted Device

**P-DSO-8-1 (SMD)**  
(Plastic Dual Small Outline)



- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Lead width can be 0.61 max. in dambar area

GPS05121

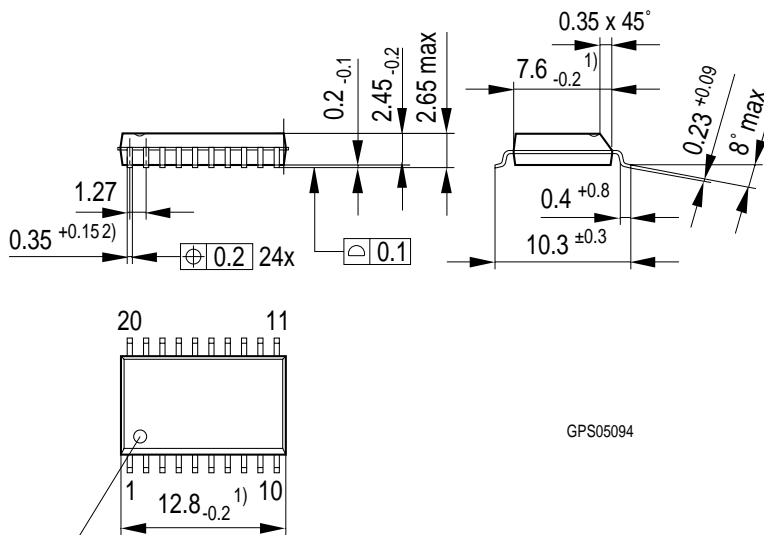
**Sorts of Packing**

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SMD = Surface Mounted Device

Dimensions in mm

**P-DSO-20-6 (SMD)**  
(Plastic Dual Small Outline)



GPS05094

Index Marking

- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.05 max per side

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

Dimensions in mm

SMD = Surface Mounted Device