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ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

TDA9503

LINE CIRCUIT FOR TV RECEIVERS

The TDA9503 is a monolithic integrated circuit for pulse separation and line synchronisation in TV receivers. The output stage of the TDA9503 (see Fig.2) supplies signals suitable for driving transistor line output stages.

An advanced version of the well-known type TBA950, the TDA9503 comprises the sync. separator with internal noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity and change of the slope of the phase control circuit, the line oscillator with frequency range limiter, a high-gain phase control circuit, a stage for generating the burst gate pulse in colour TV receivers, an undervoltage protection circuit and the output stage.

Due to the large scale of integration, or few external components are needed. The IC delivers prepared frame sync. pulses for triggering the frame oscillator. The phase comparator may be switched for video recording operation. A terminal (pin 14) for phase correction with the aid of the frame parabola is provided.

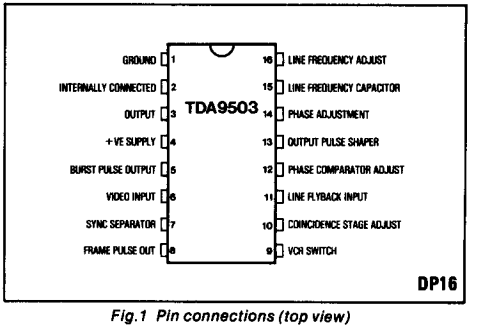

Fig.1 Pin connections (top view)

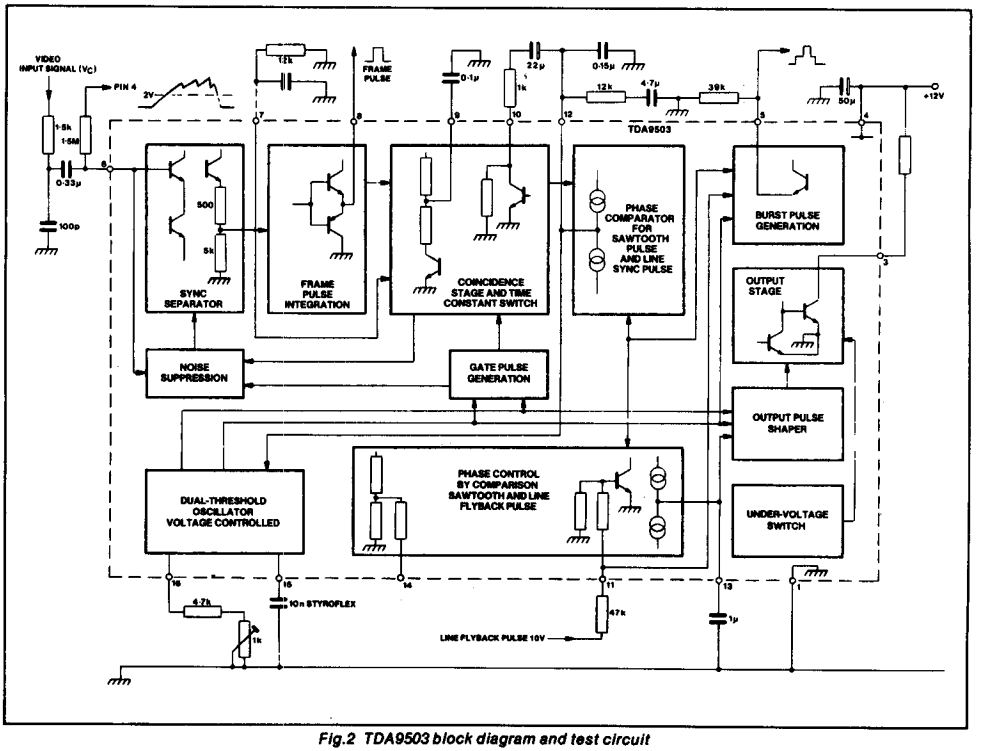

Fig.2 TDA9503 block diagram and test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_4 = 12V, f_o = 15625Hz, T_A = 25°C in the test circuit Fig.2.

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_4	9		13	V	Pin 7 unloaded
Current consumption	I_4	—	38	45	mA	
Pin 7						
Amplitude of sync signal	V_7	9	—	—	V	
Output resistance (high level)	R_{A7}	—	500	—	Ω	
Threshold for frame pulses occurring at Pin 8	V_{7th}	—	2	—	V	
Pin 8						
Amplitude of the frame sync pulses	V_8	10	—	—	V	I_8 = ±2mA
Output resistance	R_{A8}	—	—	100	Ω	
Frame pulse duration	t_8	150	—	350	µs	Pin 7 unloaded
	t_8	300	—	650	µs	Pin 7 connected to ground via 1.2kΩ//0.33µF
Delay between leading edge of frame sync pulse at Pin 6 and output signal at Pin 8	t_{V8}	—	11	—	µs	Pin 7 unloaded
	t_{V8}	—	40	—	µs	Pin 7 connected to ground via 1.2kΩ//0.33µF
Pins 2 and 3						
Output transistor saturation voltage	$V_{3/1}$	—	—	0.5	V	220Ω from Pin 3 to +12V
Output pulse duration	t_3	23.5	26	28.5	µs	See Fig.3
Pin 5						
Burst gate pulse amplitude	V_{5B}	10	—	—	V	See Fig.3
Phase shift between centre of sync pulse and leading edge of burst gate pulse	t_{B1}	2.15	2.65	3.15	µs	
Burst gate pulse duration	t_5	3.7	4	4.3	µs	
Line blanking pulse amplitude	V_{5Z}	4	4.5	5	V	See Fig.3
Oscillator frequency	f_o	15625 ± 800			Hz	C15/1 = 10nF, R16/1 = 5.1kΩ
Frequency pull-in and holding range	±Δf	650	—	1200	Hz	
Slope of phase control loop	$\frac{t_d}{t_{SR}}$	100	—	—	—	
Slope of the phase comparator loop	$\frac{f}{t_{SR}}$	—	2	—	kHz/µs	
Phase shift between sync pulse of the video signal and the line flyback pulse	t_{SR}	2.1	2.6	3.1	µs	t_d = 5µs (see Fig.3)

RECOMMENDED OPERATING CONDITIONS

	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_4	—	12	—	V
Input current during sync pulse	I_6	15	—	100	µA
Video signal input	V_6	1	3	6	V_{p-p}
Input switching current for internal noise suppression	I_{5s}	0.5	—	—	mA
Input current during line flyback pulse	I_{11}	0.1	—	2	mA
Switching current for VCR operation	I_9	2	—	—	mA
Input current (e.g. for frame parabola)	I_{14}	-50	—	50	µA
Ambient operating temp. range	T_A	0	—	60	°C

OPERATING NOTES

The sync separator separates the synchronising pulses from the composite colour video signal. The noise inverter circuit, which needs no external components, and an internal gate circuit free the sync signal from distortion.

The frame sync pulse is obtained by internal integration and limitation of the sync signal, and is available at pin 8. The typical delay time between the leading edge of the frame sync pulses at pin 6 and the output signal at pin 8 amounts to 11μs. This time can be enlarged by means of an external RC combination connected to pin 7, which integrates the separated frame sync pulses, before they are given to the input of the following threshold switch. The latter has a threshold of 2V.

The frequency of the line oscillator is determined by a 10nF Styroflex capacitor at pin 15 which is charged and discharged periodically by two internal current sources. The external resistor at pin 16 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync pulse. Simultaneously an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the line flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The normal phase position is obtained if pin 14 is open-circuit. Any phase displacement can be corrected by a current or voltage fed into pin 14. The duration of the output pulse is thereby not influenced.

The burst gate pulse is derived from the sawtooth voltage of the line oscillator and therefore via the phase comparator synchronised with the line sync pulses of the colour video signal.

The switching stage has different functions. When the two signals supplied by the sync separator and the phase control circuit respectively are in synchronism a saturated transistor is in parallel with the integrated 2kΩ resistor at pin 10. Thus the time constant of the filter network at pin 12 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronised state. This arrangement ensures distrubance-free operation. Moreover, because the internal noise suppression and the internal gate circuit in synchronised operation are effective, the noise limitation is improved.

For video recording operation the automatic switchover can be blocked by a positive current fed into pin 9, e.g. via a resistor connected to pin 4. This reduces the time constant at pin 12 and increases the control current of the phase comparator thus steepening the static slope of the phase comparator which gives optimised matching in video recording operation.

The output transistor of the TDA9503 is operated in common emitter configuration. Its output current is limited to 50mA by the pull-up resistor between pin 3 and the supply voltage. This current serves for driving the line deflection driver transistor.

If the supply voltage goes down (e.g. by switching off the mains) a built-in protection circuit ensures defined line frequency pulses down to V_4= 4V and shuts off when V_4 falls below 4V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as V_4 reaches 4.5V. In the range between V_4 = 4.5V and full supply voltage the shape and frequency of the output pulses are practically constant.

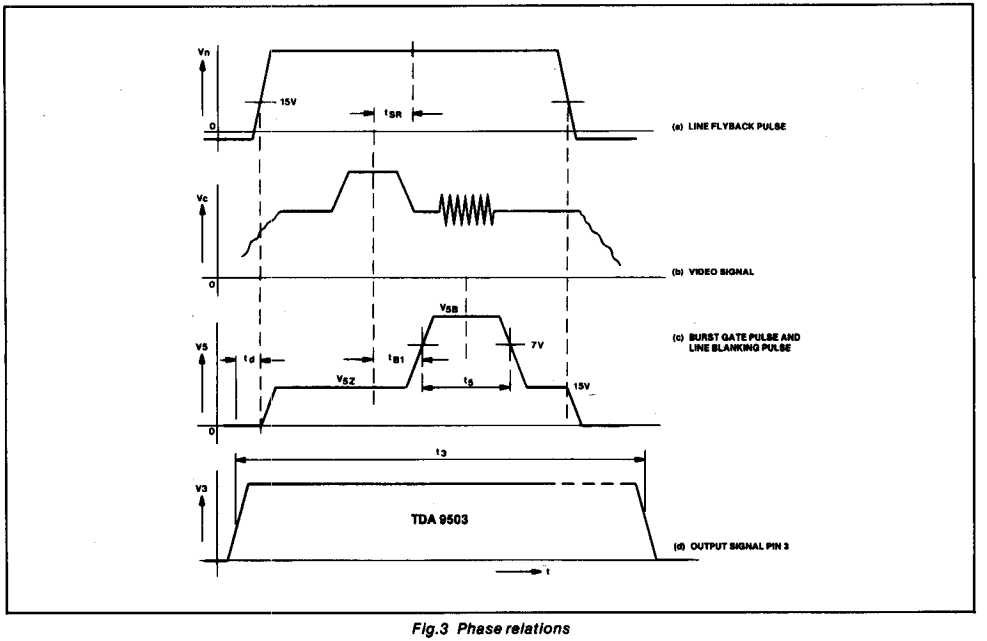

Fig.3 Phase relations

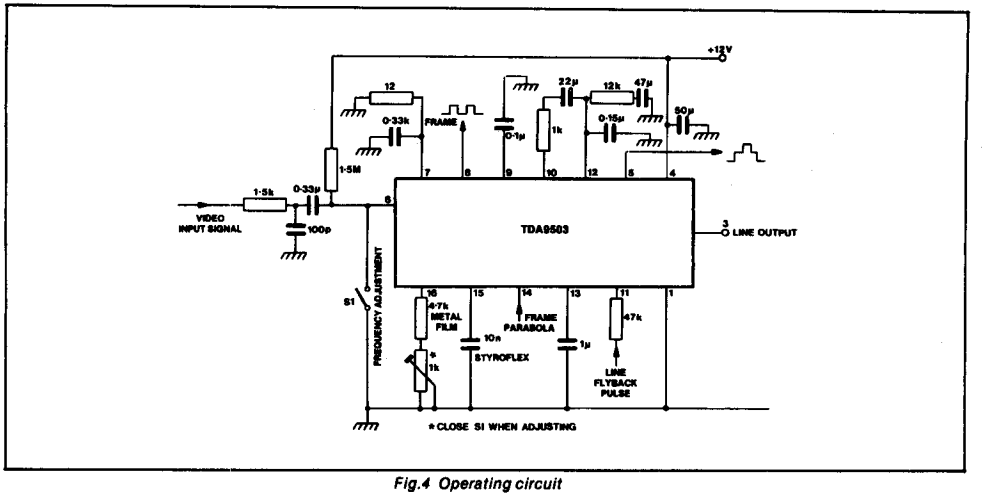

Fig.4 Operating circuit

ABSOLUTE MAXIMUM RATINGS

	Symbol	Value	Unit
Supply voltage	V_4	14	V
Input voltage	V_6	−6	V
Output voltages	V_3	20	V
Output currents	I_6	−20	mA
	$\pm I_6$	20	mA
	I_3	50	mA
Input currents	I_{11}	5	mA
	I_9	5	mA
Operating temperature range	T_A	−10 to +60	°C
Storage temperature range	T_S	−55 to +125	°C