

DATA SHEET

TDA8354Q

Full bridge current driven vertical
deflection output circuit in LVDMOS

Preliminary specification
File under Integrated Circuits, IC02

1998 Sep 03

Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Short rise and fall times of the vertical flyback switch
- Guard circuit
- Temperature (thermal) protection
- High ElectroMagnetic Compatibility (EMC) because of common mode inputs
- Guard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8354Q is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 25 to 200 Hz and 16 : 9 picture tubes. The circuit provides a DC-driven vertical deflection output circuit, operating as a highly efficient class G system. Due to the full bridge output circuit the deflection coils can be DC coupled.

The IC is constructed in a low-voltage DMOS process that combines bipolar, CMOS and DMOS devices, to provide ruggedness.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	supply voltage		7.5	12	18	V
$I_{Q(av)}$	average quiescent supply current	during scan	–	10	15	mA
V_{flb}	flyback supply voltage		$2 \times V_P$	45	68	V
$I_{Vflb(av)}$	average flyback supply current	during scan	–	–	10	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		–	–	3.2	A
$I_{i(diff)(p-p)}$	input current (peak-to-peak value) at pin 11 or 12		–	500	600	µA
Flyback switch						
$I_{O(Vflb)}$	peak output current	$t \leq 1.5$ ms	–	–	±1.6	A
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		–25	–	+75	°C
T_j	junction temperature		–	–	150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8354Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

Full bridge current driven vertical deflection
output circuit in LVDMOS

TDA8354Q

BLOCK DIAGRAM

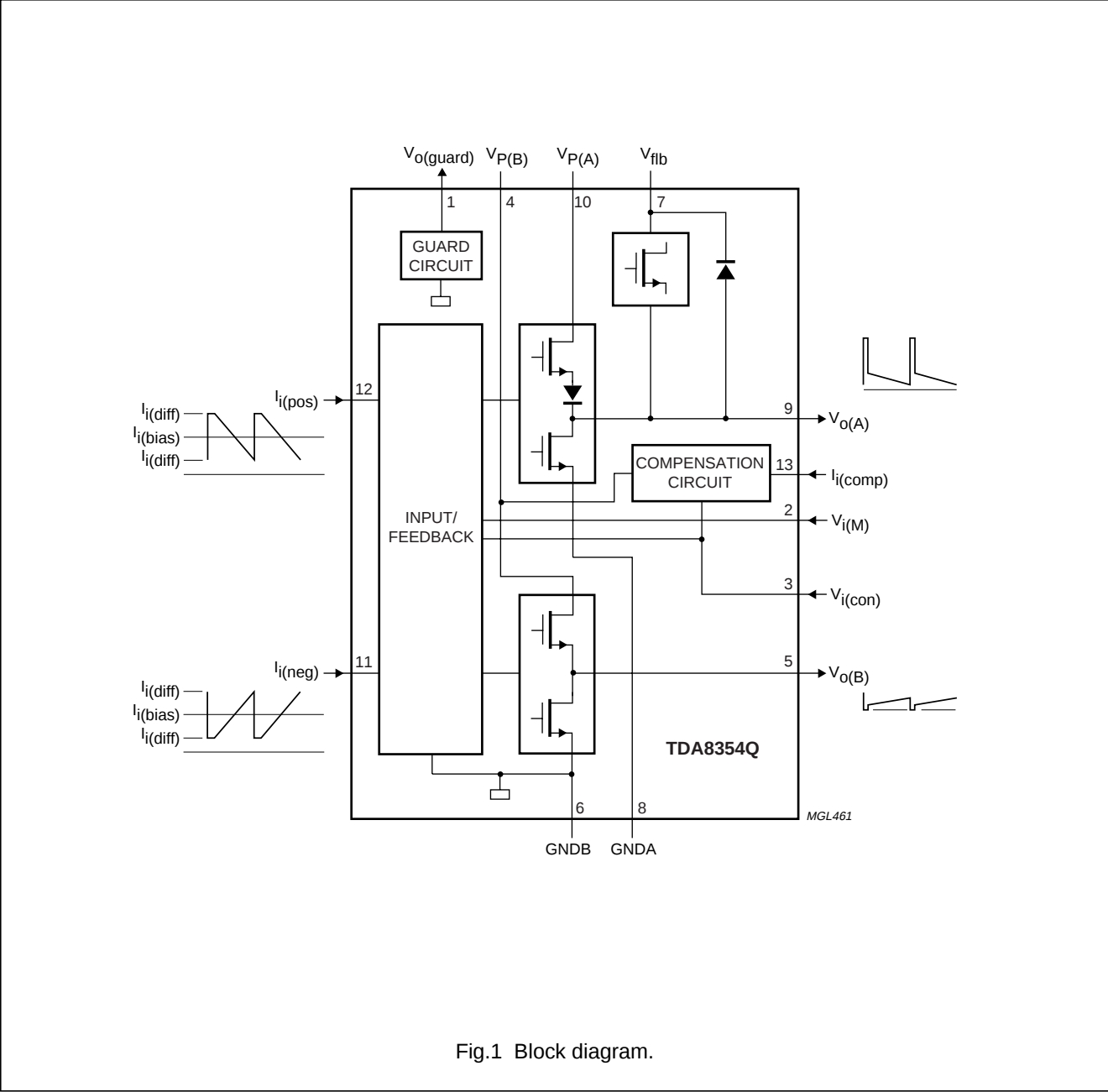


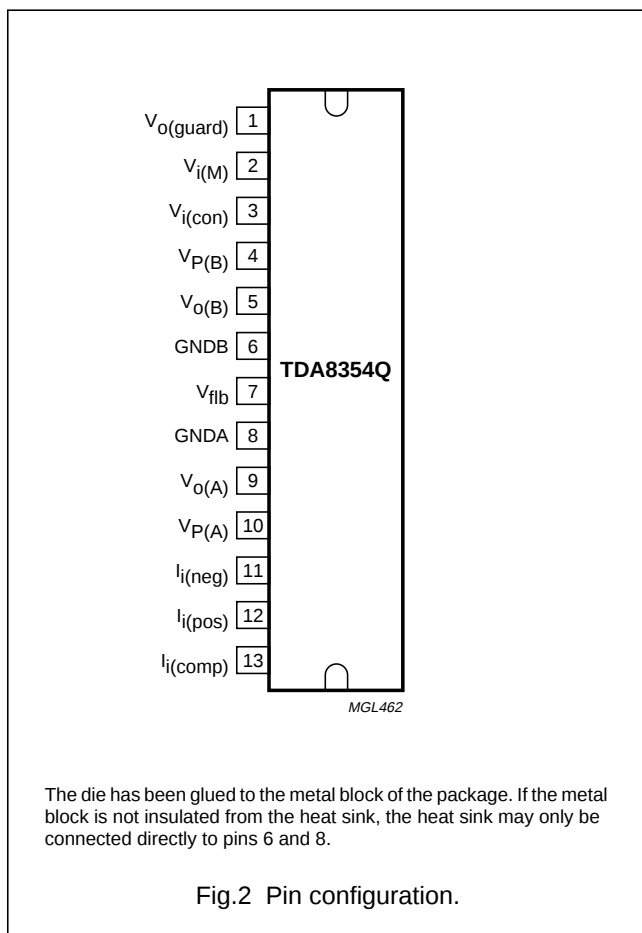
Fig.1 Block diagram.

Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{o(\text{guard})}$	1	guard output voltage
$V_{i(M)}$	2	measuring resistor input
$V_{i(\text{con})}$	3	conversion resistor input
$V_{P(B)}$	4	supply voltage B
$V_{o(B)}$	5	output voltage B
GNDB	6	ground B
V_{flb}	7	flyback supply voltage
GNDA	8	ground A
$V_{o(A)}$	9	output voltage A
$V_{P(A)}$	10	supply voltage A
$I_{i(\text{neg})}$	11	input power-stage (negative); includes $I_{i(\text{bias})}$ signal bias
$I_{i(\text{pos})}$	12	input power-stage (positive); includes $I_{i(\text{bias})}$ signal bias
$I_{i(\text{comp})}$	13	damping resistor compensation current input



FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. The differential input circuit is current driven. The input circuit is special intended for direct connection to driver circuits which deliver symmetrical current signals, but is also suitable for asymmetrical currents. The current to voltage conversion is done by the external resistor (R_{con}) connected between the output of the input conversion stage and output stage B. This voltage is compared with the output current through the deflection coil measured as voltage across R_M , which provides internal feedback information. The relationship between the differential input current and the output current is defined by:

$$2 \times I_{i(\text{diff})} \times R_{\text{con}} = I_{\text{coil}} \times R_M$$

The output current is adjustable from 0.5 A (p-p) to 3.2 A (p-p) by varying R_{con} . The maximum input current is 800 μA peak for each pin. The minimum input current should be 50 μA .

Flyback supply

The flyback voltage is determined by an additional supply voltage V_{flb} . The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{flb} optimum for the flyback voltage. Using this method, very high efficiency is achieved. The supply voltage V_{flb} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a coupling capacitor (not necessary, due to the bridge configuration). The very short rise and fall time of the flyback switch is $>400 \text{ V}/\mu\text{s}$.

Protection

The output circuit has protection circuits for:

- Die temperature control
- Overvoltage of output stage A.

Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

Guard circuit

A guard circuit with output signal $V_{o(\text{guard})}$ is provided.

The guard circuit generates an active HIGH level during the flyback period. The guard circuit is also activated for one or more of the following conditions:

- When the thermal protection is activated ($T_j \approx 170^\circ\text{C}$)
- During short-circuit of the output pins (pins 5 and 9) to V_P or ground
- During open coil
- During open loop
- During short-circuit of the input pins (pins 11 and 12) to V_P or ground.

An active HIGH level of the guard signal is also generated for the next conditions:

- No drive signal
- Short-circuit of the coil.

However, for these events the signal is generated via an internal timer circuit. The guard signal set via this timer has a delay of ≈ 120 ms. The delay time is given by the lowest applicable field frequency.

The guard signal can be used for blanking the picture tube screen and signalling a fault condition.

Damping resistor compensation

For HF-loop stability a damping resistor is connected across the deflection coil. There is a big difference in current in the damping resistor R_p during scan and flyback. The resistor current is summed to the current in the deflection coil via the measuring resistor R_M , which results in a too low current in the deflection coil at the start of the scan.

To reach a short settling time the difference in the current during scan and flyback in the damping resistor can be compensated for by external means. To do so a resistor (R_{comp}) of about $1\text{ M}\Omega$ can be connected between the output of stage A (pin 9) and the damping resistor compensation current input (pin 13).

For a more accurate calculation of R_{comp} refer to the following formula:

$$R_{\text{comp}} = \frac{(V_{\text{flb}} - V_{\text{loss}} - V_P) \times R_p \times R_{\text{con}}}{(V_{\text{flb}} - V_{\text{loss}} - I_L \times R_L) \times R_M}$$

Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
DC supply					
V_P	supply voltage		–	18	V
V_{flb}	flyback supply voltage		–	68	V
Vertical circuit					
$I_{o(p-p)}$	output current (peak-to-peak value)		–	3.2	A
$V_{o(A)}$	output voltage (pin 9)	note 1	–	68	V
$V_{o(B)}$	output voltage (pin 5)		–	V_P	V
$I_{1,2,3,11,12,13}$	current into or out of pins 1 to 3 and 11 to 13		–20	+20	mA
$V_{1,2,3,11,12,13}$	peak voltage on pins 1 to 3 and 11 to 13		–0.5	V_P	V
Flyback switch					
$I_{o(Vflb)}$	peak output current		–	± 1.6	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_j	junction temperature	note 2	–	150	°C
Miscellaneous					
t_{sc}	short-circuiting time	note 3	–	1	h
$I_{i/o}$	current into any pin	$+1.5 \times V_{P(max)} $; note 4	–	+200	mA
	current out of any pin	$-1.5 \times V_{P(max)} $; note 4	–200	–	mA
V_{ESD}	electrostatic handling	note 5	–	± 300	V
		note 6	–	± 2000	V

Notes

- When the pin voltage exceeds 70 V the device behaves like a power zener diode thus limiting the voltage.
- Internally limited by thermal protection; switching point ≈ 170 °C.
- Up to $V_P = 18$ V.
- At $T_{j(max)}$.
- Machine model: equivalent to discharge a 200 pF capacitor through a 0 Ω series resistor. Except pin 7: ± 250 V.
- Human body model: equivalent to discharge a 100 pF capacitor through a 1.5 k Ω series resistor. Except pin 7: ± 1500 V.

Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case		4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

CHARACTERISTICS

$V_P = 12\text{ V}$; $V_{flb} = 45\text{ V}$; $f_i = 50\text{ Hz}$; $I_{i(bias)} = 330\text{ }\mu\text{A}$; $T_{amb} = 25\text{ }^\circ\text{C}$; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supply						
V_P	operating supply voltage		7.5	12	18	V
V_{flb}	flyback supply voltage		$2 \times V_P$	45	68	V
$I_{q(av)}$	average quiescent supply current	during scan	–	10	15	mA
I_q	quiescent supply current	no signal; no load	–	60	80	mA
$I_{vflb(av)}$	average flyback supply current	during scan	–	–	10	mA
Output stage A and B						
V_{loss}	voltage loss from pin 10 to 9 and from pin 5 to 6	$I_o = 3.2\text{ A (p-p)}$; note 1	–	–	6.0	V
	voltage loss from pin 4 to 5 and from pin 9 to 8		–	–	4.8	V
	voltage loss from pin 10 to 9 and from pin 5 to 6	$I_o = 2.2\text{ A (p-p)}$; note 1	–	–	4.2	V
	voltage loss from pin 4 to 5 and from pin 9 to 8		–	–	3.4	V
LE	linearity error					
	adjacent blocks	$I_o = 3.2\text{ A (p-p)}$; note 2	–	0.5	2	%
	not adjacent blocks	$I_o = 3.2\text{ A (p-p)}$; note 2	–	0.5	3	%
V_o	output voltage swing (flyback) $V_{o(A)} - V_{o(B)}$	$I_{i(diff)} = 0.3\text{ mA}$; $I_o = 1.6\text{ A}$	–	46	–	V
$ V_{offset} $	offset voltage across R_M	$I_{i(diff)} = 0$ $I_{i(bias)} = 500\text{ }\mu\text{A}$ $I_{i(bias)} = 100\text{ }\mu\text{A}$	– –	– –	15 13	mV mV
$\Delta V_{offset(T)}$	offset voltage as function of temperature	$I_{i(diff)} = 0$	–	–	40	$\mu\text{V/K}$
$V_{o(A)}, V_{o(B)}$	DC output voltage	$I_{i(diff)} = 0$; note 3	–	$\frac{V_P}{2}$	–	V
$G_{v(ol)}$	open-loop voltage gain $V_{9\text{ to }5}/V_{3\text{ to }5}$	notes 4 and 5	–	60	–	dB
$V_{3\text{ to }5}/V_{2\text{ to }5}$	voltage ratio $V_{3\text{ to }5}/V_{2\text{ to }5}$	note 4	–	0	–	dB
f_{res}	frequency response (–3 dB)	open loop	–	1	–	kHz
G_i	current gain ($I_o/I_{i(diff)}$)		–	8000	–	

Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_{i(T)}$	current gain drift as function of temperature		–	–	10^{-4}	/K
PSRR	power supply rejection ratio	note 6	80	90	–	dB
Input stage						
$I_{i(bias)}$	signal bias current		–	330	500	μA
$I_{i(diff)(p-p)}$	differential mode input current (peak-to-peak value) pin 11 or 12	note 7	–	500	600	μA
$V_{i(diff)}$	differential mode input voltage	$I_{i(diff)} = 500 \mu A$	–	0.75	–	V
$V_{i(cm)}$	common mode input voltage	$I_{i(bias)} = 330 \mu A$	0.95	1.15	1.35	V
Flyback switch						
$I_{o(V_{flb})}$	output peak current	$t < 1.5 \text{ ms}$	–	–	± 1.6	A
V_{loss}	voltage loss ($V_{flb} - V_{o(A)}$)	$I_o = +1.6 \text{ A}$	–	8	9	V
Guard circuit						
$I_{o(guard)}$	output current	not active; $V_{o(guard)} = 0 \text{ V}$	–	–	10	μA
		active; $V_{o(guard)} = 4.5 \text{ V}$	1	–	2.5	mA
$V_{o(guard)}$	output voltage on pin 1	$I_{o(guard)} = 100 \mu A$	5	6	7	V
	allowable voltage on pin 1	maximum leakage current = $10 \mu A$	–	–	18	V

Notes

- At $T_j = 125^\circ \text{C}$. The temperature coefficient of V_{loss} has a positive sign.
- The linearity error is measured without S correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
Divide the output signal into 22 equal time parts ranging from 1 to 22 inclusive. Measure the value of the voltage across R_M of two succeeding parts called one block (a) starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus parts 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and not adjacent blocks (LENAB) are given below:

$$LEAB = \frac{a_k - a_{(k+1)}}{a_{av}}$$

$$LENAB = \frac{a_{max} - a_{min}}{a_{av}}$$
- $V_{o(A)} + V_{o(B)} = V_P$. At the start of the scan this equation is one diode voltage less.
- The V value within formulae relates to voltages at or between relative pin numbers, i.e. $V_{9 \text{ to } 5} / V_{3 \text{ to } 5}$ = voltage value across pins 9 and 5 divided by voltage value across pins 3 and 5.
- $V_{2 \text{ to } 5}$ AC short-circuited.
- At $V_{(ripple)} = 500 \text{ mV (eff)}$ at V_P ; measured across R_M ; $f_{(ripple)} = 50 \text{ Hz} - 1 \text{ kHz}$.
- $I_{i(bias)} + I_{i(diff)} \leq 800 \mu A$ and $I_{i(bias)} - I_{i(diff)} \geq 50 \mu A$ per pin.

Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

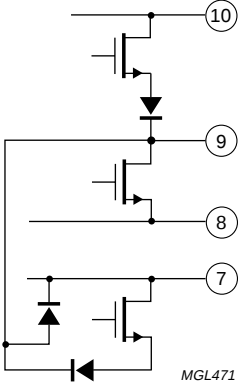
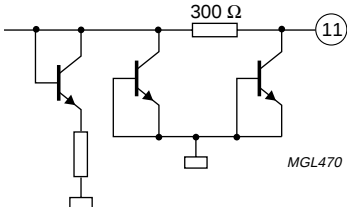
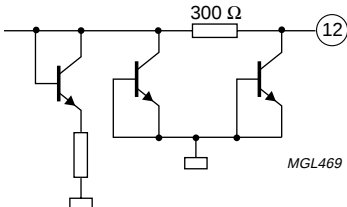
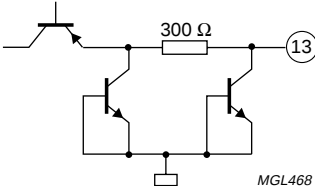
INTERNAL CIRCUITRY

Table 1 Equivalent pin circuits

PIN	SYMBOL	EQUIVALENT CIRCUIT
1	$V_{o(\text{guard})}$	MGL472
2	$V_{i(\text{M})}$	MGL465
3	$V_{i(\text{con})}$	MGL466
4	$V_{P(\text{B})}$	MGL467
5	$V_{o(\text{B})}$	
6	GNDB	

Full bridge current driven vertical deflection
output circuit in LVDMOS

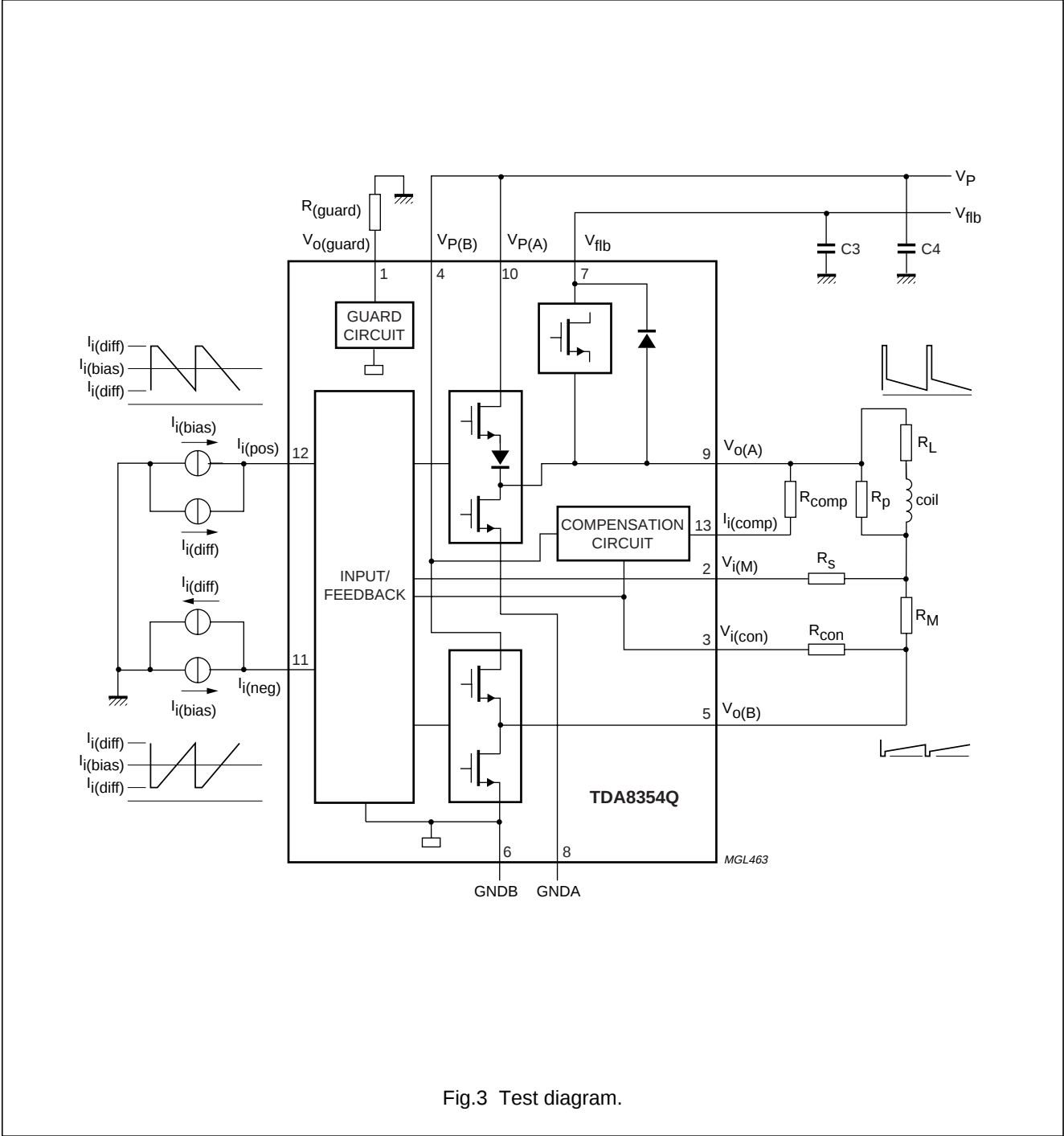
TDA8354Q

PIN	SYMBOL	EQUIVALENT CIRCUIT
7	V_{filb}	
8	GNDA	
9	$V_{o(A)}$	
10	$V_{P(A)}$	
11	$I_{i(neg)}$	
12	$I_{i(pos)}$	
13	$I_{i(comp)}$	

Full bridge current driven vertical deflection
output circuit in LVDMOS

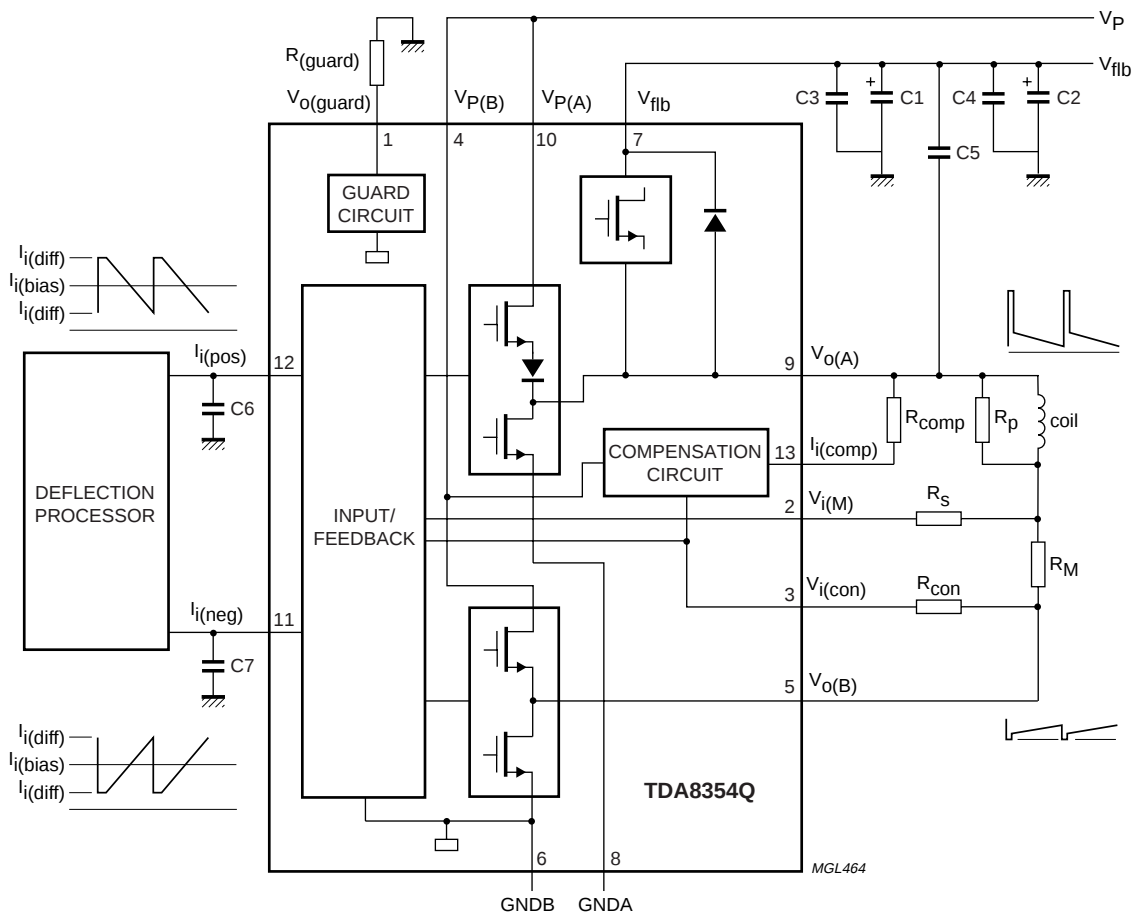
TDA8354Q

TEST AND APPLICATION INFORMATION



Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q



Coil: AT6216/42;
 $V_P = 12.1 \text{ V}$ at $f_v = 50 \text{ Hz}$ (vertical frame frequency); inclusive spread (absolute) and temperature rise in the coil;
 $V_P = 12.8 \text{ V}$ at $f_v = 100 \text{ Hz}$ (vertical frame frequency); inclusive spread (absolute) and temperature rise in the coil;
 $I_{O(p-p)} = 2.33 \text{ A}$ (peak-to-peak);
 $I_{i(\text{bias})} = 330 \mu\text{A}$;
 $I_{i(\text{diff})(12-11)} = 485 \mu\text{A}$ (peak value);
 $V_{flb} = 45 \text{ V}$;
 $t_{flb} = 0.6 \text{ ms}$.

$R_M = 0.5 \Omega$;
 $R_{con} = R_S = 1.2 \text{ k}\Omega$;
 $R_P = 300 \Omega$;
 $R_{comp} = 650 \text{ k}\Omega$;
 $R_{guard} = 5 \text{ k}\Omega$.

$C_1 = 47 \mu\text{F}$; 100 V ;
 $C_2 = 220 \mu\text{F}$; 25 V ;
 $C_3 = C_4 = 100 \text{ nF}$;
 $C_5 = 10 \text{ nF}$;
 $C_6 = C_7 = 10 \text{ nF}$.

Fig.4 Application diagram.

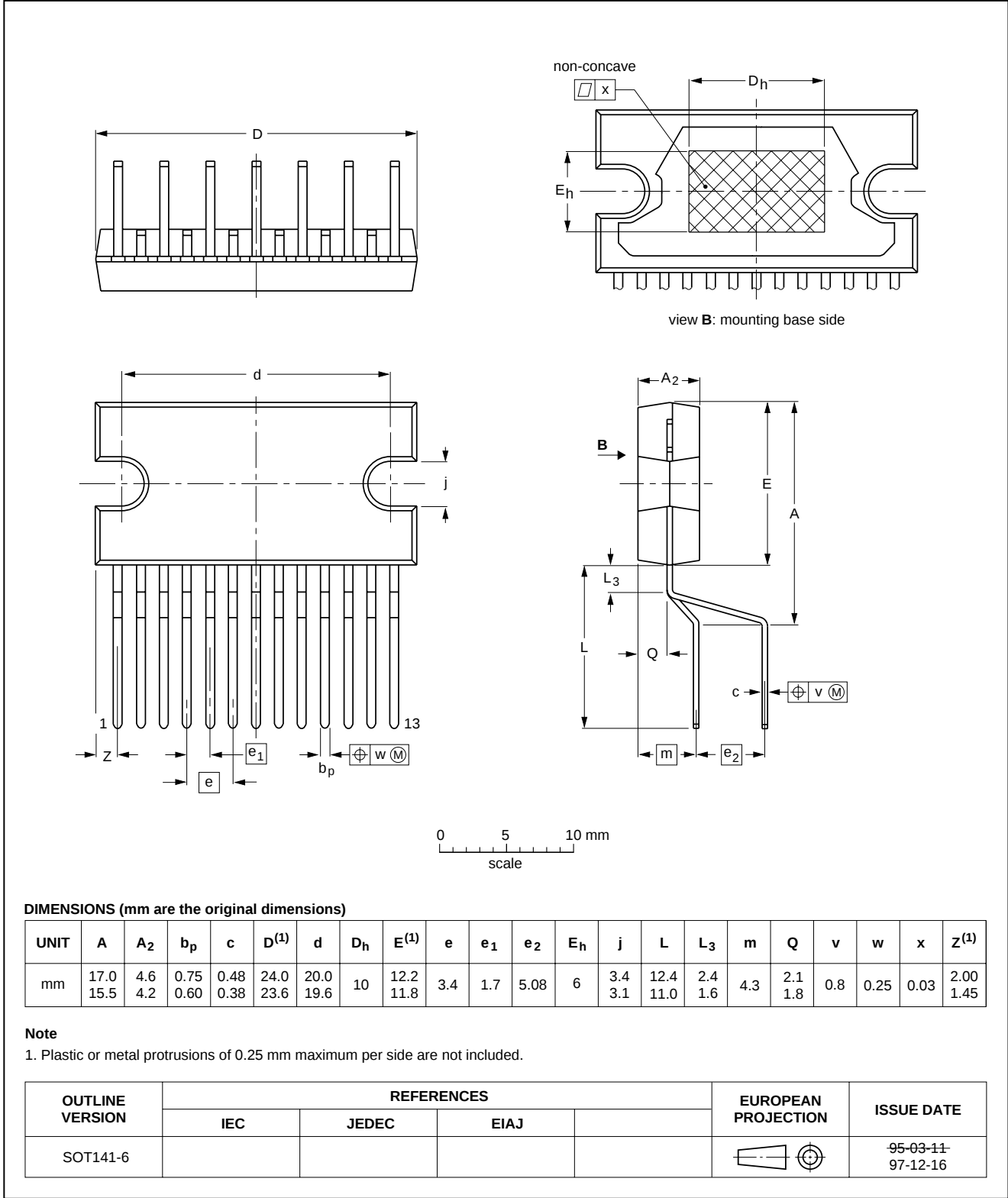
Full bridge current driven vertical deflection
output circuit in LVDMOS

TDA8354Q

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)

SOT141-6



Full bridge current driven vertical deflection output circuit in LVDMOS

TDA8354Q

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Full bridge current driven vertical deflection
output circuit in LVDMOS

TDA8354Q

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 1998

SCA60

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

545104/00/01/pp16

Date of release: 1998 Sep 03

Document order number: 9397 750 04083

Let's make things better.

**Philips
Semiconductors**



PHILIPS