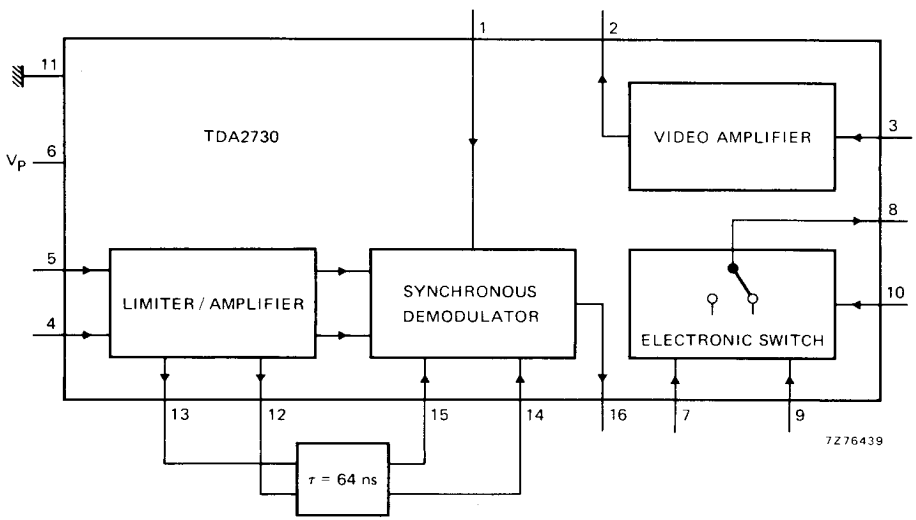
FM LIMITER/DEMODULATOR

The TDA2730 is a monolithic integrated circuit for use in audio-visual equipment, e.g.: video recorders and video disc players.
The circuit comprises an f.m. limiter/demodulator for the playback signal, a video amplifier and an electronic switch, which can be used for drop-out elimination.

QUICK REFERENCE DATA				
Supply voltage	V_{6-11}	typ.	12	V
Supply current	I_6	typ.	42	mA
Input signal range (peak-to-peak value)	$V_{4-5(p-p)}$		30 to 2000	mV
Video output signal (peak-to-peak value)	$V_{2-11(p-p)}$	typ.	4	V

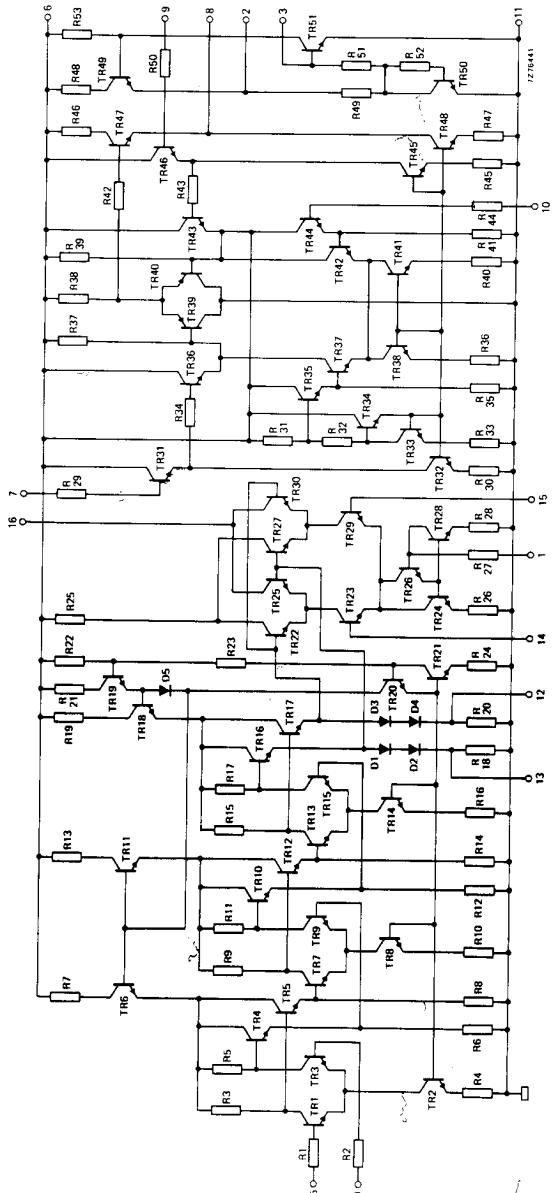
BLOCK DIAGRAM



PACKAGE OUTLINE

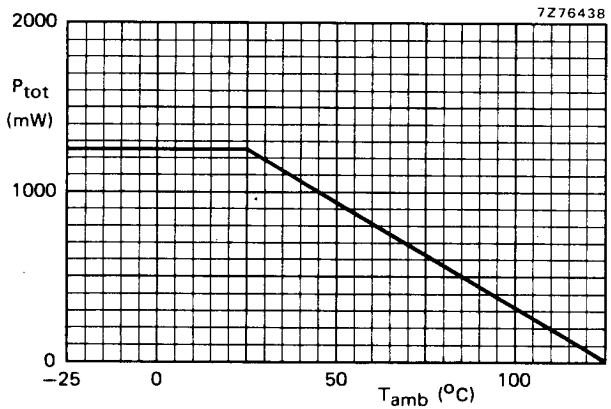
16-lead DIL: plastic (SOT-38).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Supply voltage	V_{6-11}	max.	13	V
Power dissipation				
Total power dissipation (see also derating curve below)	P_{tot}	max.	1,25	W
Temperatures				
Storage temperature	T_{stg}		−65 to +125	°C
Operating ambient temperature			see derating curve below	



CHARACTERISTICS measured in the circuit on page 7 (Fig. 1)

Supply voltage range	V_{6-11}	typ. 12	V
		11 to 13	V

The following characteristics are measured at V_{6-11} = 12 V; T_{amb} = 25 °C

Supply current	I_6	typ. 42	mA
		25 to 54	mA

Limiter

Start of limiting (−3 dB) f_o = 4 MHz; peak-to-peak value	$V_{4-5(p-p)}$	typ. 0,8	V
Input signal range for constant luminance output (peak-to-peak value)	$V_{4-5(p-p)}$	30 to 2000	mV
Output voltage (peak-to-peak value)	$V_{12-13(p-p)}$	typ. 750	mV
Available output voltage at an external load of 1 kΩ; peak-to-peak value	$V_{12-13(p-p)}$	> 5	V

Demodulator

Measured at I_1 = 4 mA; $|Z_{16-11}|$ = 1,5 kΩ; delay time τ = 64 ns; Δf = 1,4 MHz (f_L = 3,0 MHz, f_H = 4,4 MHz)

Current ratio	I_1/I_{16}	typ. 1	
Output voltage (peak-to-peak value)	V_{16-11}	typ. 540	mV

Drop-out switch

Input drive voltage range	$V_{7;9-11}$	6,5 to 12	V
Voltage drop between input and output for signal flow from pin 7 to pin 8	V_{7-8}	typ. 1,5	V
for signal flow from pin 9 to pin 8	V_{9-8}	typ. 1,5	V
Input offset voltage	$\lvert V_{7-8}-V_{9-8}\rvert$	< 20	mV
Switch actuating input voltage for signal flow from pin 7 to pin 8	V_{10-11}	0 to 2,7	V
for signal flow from pin 9 to pin 8	V_{10-11}	3,7 to 6,0	V
Output impedance at 1,5 mA by internal load	Z_{8-11}	emitter follower	

CHARACTERISTICS (continued)

Video amplifier

Input voltage level	V_{3-11}	typ.	730	mV
Output voltage level	V_{2-11}	typ.	5,5	V
Open loop gain	G	typ.	43	dB
Bandwidth (3 dB)	B	typ.	8,8	MHz
Output voltage (peak-to-peak value; see note)	$V_{2-11(p-p)}$	typ.	4	V

Note

The gain of the amplifier is determined by the feedback network comprising the impedances between pins 2 and 3, and pins 8 and 3. The values quoted apply to the circuit on page 7 (Fig. 1).

PINNING

1. Current setting demodulator
2. Video amplifier output
3. Video amplifier input
4. F.M. signal input
5. F.M. signal input
6. Positive supply
7. Switch input
8. Switch output
9. Switch input
10. Switch actuating input
11. Negative supply (ground)
12. Limiter output
13. Limiter output
14. Demodulator input
15. Demodulator input
16. Demodulator output

APPLICATION INFORMATION

The function is quoted against the corresponding pin number

1. Current setting of demodulator

   The current into this pin directly **determines** the amplitude and the d.c. level of the demodulator output. At I_1 = 4 mA, optimum temperature compensation is obtained.

2. Video amplifier output

   A signal up to 4 V peak-to-peak is available from this output (Fig. 1).
   This can be the video signal (Fig. 1) or the f.m. signal to the delay line (drop-out elimination; Fig. 2).

3. Video amplifier input

   The demodulator output signal is the input signal to this pin (Fig. 1) or the f.m. modulated signal (Fig. 2).

4. F.M. signal input (in conjunction with pin 5)

   A frequency modulated signal of 1 V peak-to-peak is applied between pins 4 and 5.
   D.C. feedback from the limiter output is applied to stabilize the operation.

5. F.M. signal input

   See pin 4.

APPLICATION INFORMATION (continued)

6. Positive supply

   Correct operation can be obtained in the range 11 to 13 V.

7. Switch input

   The signal applied to pin 7 or to pin 9 is transferred to pin 8, depending on the switch position. For an input level between 0 and 2,7 V at pin 10, the signal at pin 7 is transferred to pin 8, and when between 3,7 and 6 V the input signal at pin 9 is transferred to pin 8.
   The signal at pin 7 or pin 9 may vary from 6,5 to 12 V.
   The signal at pin 8 is 1,5 V below the value at pin 7 or 9.
   The difference in input level at pins 7 and 9, to obtain equal output at pin 8, will be less than 20 mV.

8. Switch output

   See pin 7.

9. Switch input

   See pin 7.

10. Switch actuating input

    See pin 7.

11. Negative supply (ground)

12. Limiter output

    A balanced signal is available between pins 12 and 13. The signal amplitude is limited to 750 mV at both outputs.

13. Limiter output

    See pin 12.

14. Demodulator input

    A phase shifted signal (with respect to the internally applied signal) is applied between pins 14 and 15.

15. Demodulator input

    See pin 14.

16. Demodulator output

    The output signal is proportional to :
    - current into pin 1
    - slope of the phase characteristic of the network between pins 12 and 13, and pins 14 and 15
    - impedance level at the output
    - the sweep (Δf) of the f. m. signal.

    A signal of typically 540 mV is available at this pin when using the component values in Fig. 1 and Δf = 1,4 MHz.

APPLICATION INFORMATION (continued)

Test circuit

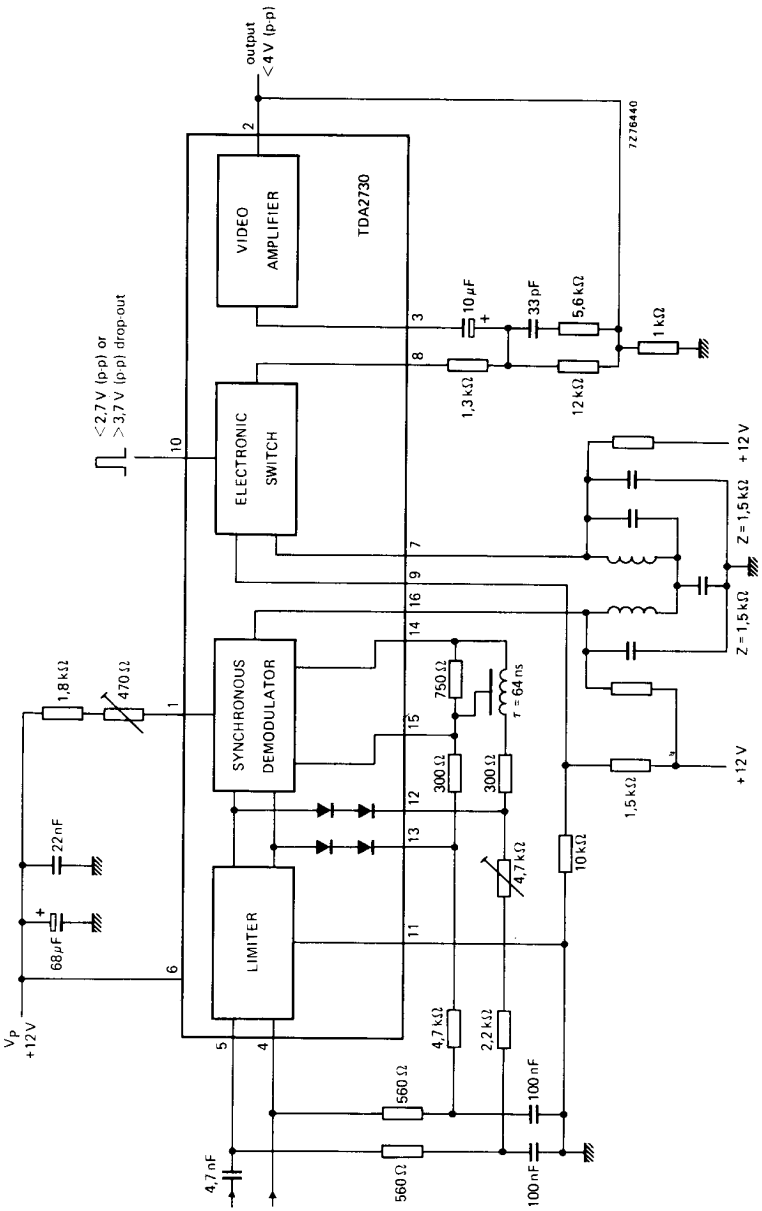


Fig. 1

APPLICATION INFORMATION (continued)

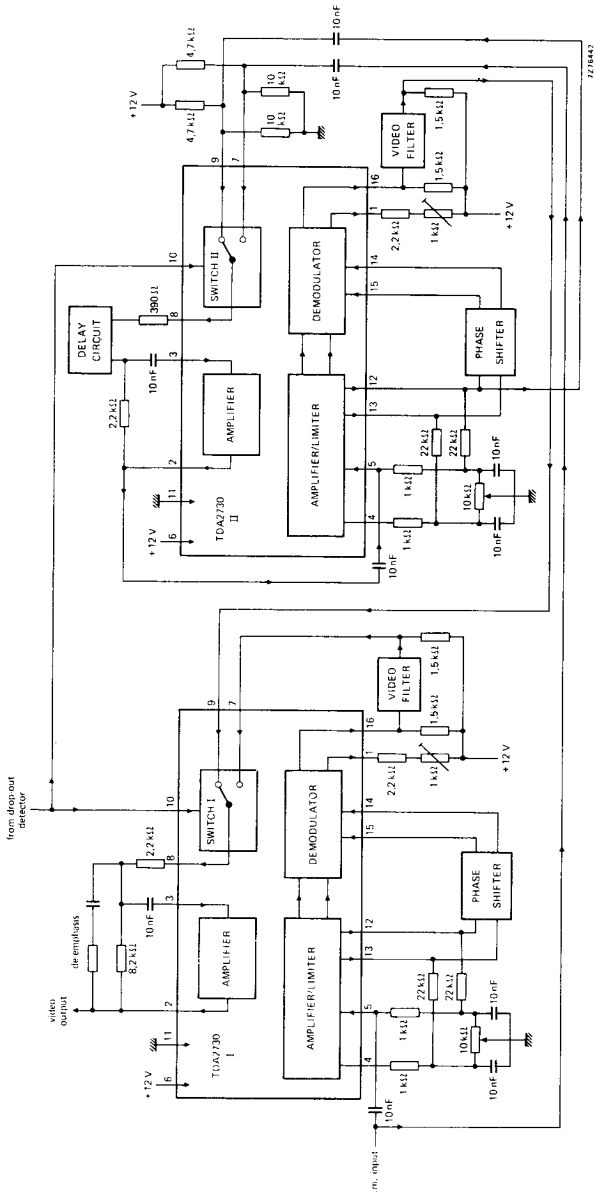


Fig. 2. Drop-out eliminator.