TAA 630S

LINEAR INTEGRATED CIRCUIT

SYNCHRONOUS DEMODULATOR FOR PAL COLOUR TV SETS

The TAA 630 S is a silicon monolithic integrated circuit in a 16-lead dual in-line plastic package. It incorporates the following functions:

— active synchronous demodulators for F (B-Y) and ± F (R-Y) signals

— matrix for G-Y signal [G-Y = -0.51 (R-Y) -0.19 (B-Y)]

— flip-flop

— PAL switch and colour killer.

It is intended for PAL colour television receivers employing colour difference output stages with clamping circuits.

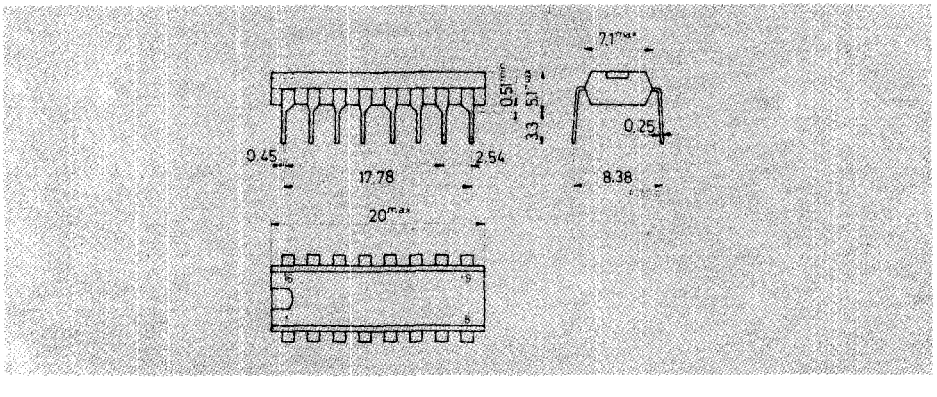
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (between pins 6 and 16 - see note)	13.2 V
V_1	Reverse identification input voltage	-5 V
I_1	Identification input current	1 mA
I_o	Output current (from pins 4, 5 and 7)	5 mA
P_{tot}	Total power dissipation: at $T_{amb} \leq 50$ °C (see note)	550 mW
T_{stg}	Storage temperature	-20 to 125 °C
T_{op}	Operating temperature	-20 to 60 °C

NOTE: $V_s = 16$ V and $P_{tot} = 800$ mW (at $T_{amb} \leq 50$ °C) are permissible during warm up time of tubes in mixed sets

MECHANICAL DATA

Dimensions in mm



ELECTRICAL CHARACTERISTICS

(measured using the test circuit of fig. 3 at $T_{amb} = 25\,°C$)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
STATIC (DC) CHARACTERISTICS						
I_1	Input current for identification circuit ON	$V_{10} \geqslant 0.9$ V			80	µA
V_1	Input voltage for identification circuit ON				0.75	V
V_1	Input voltage for identification circuit OFF				0.4	V
V_4*	DC voltage at (R-Y) output				see note	V
V_5*	DC voltage at (G-Y) output				see note	V
V_7	DC voltage at (B-Y) output				7.3	V
V_{10}	Killer input voltage for colour ON				0.9	V
V_{10}	Killer input voltage for colour OFF				0.3	V
DYNAMIC CHARACTERISTICS						
V_1	Peak to peak identification input voltage	$V_{10} \geqslant 0.9$ V f = 7.8 kHz			4	V
V_3	Peak to peak flip-flop output voltage				2.5	V
V_4	R-Y output voltage swing	$V_{10} \geqslant 0.9$ V f = 4.4 MHz Linearity m $\geqslant 0.7$			3.2	V
V_5	G-Y output voltage swing				1.8	V
V_7	B-Y output voltage swing				4	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_2**	R-Y reference input voltage	$V_{10} \geqslant 0.9$ V f = 4.4 MHz		1		V
V_8**	B-Y reference input voltage			1		V
V_{14}	Peak flip-flop input voltage	$V_{10} \geqslant 0.9$ V f = 15.6 kHz	-2.5		-5	V
V_{15}	Peak flip-flop input voltage		-2.5		-5	V
V_4/V_{13}***	R-Y demodulator gain	$V_{10} \geqslant 0.9$ V f = 4.4 MHz V_i (peak to peak) = 50 mV		7		—
$\frac{V_7}{V_9} \cdot \frac{V_{13}}{V_4}$	B-Y demodulator gain to R-Y demodulator gain ratio			1.78		—
R_9	Parallel input resistance at pin 9	$V_{10} \geqslant 0.9$ V f = 4.4 MHz V_i = 20 mV		800		Ω
C_9	Parallel input capacitance at pin 9				10	pF
R_{13}	Parallel input resistance at pin 13			800		Ω
C_{13}	Parallel input capacitance at pin 13				10	pF
$\|Z_4\|$	R-Y output impedance	$V_{10} \geqslant 0.9$ V			100	Ω
$\|Z_5\|$	G-Y output impedance				100	Ω
$\|Z_7\|$	B-Y output impedance				100	Ω
$\|Z_2\|$	Parallel input impedance at pin 2	$V_{10} \geqslant 0.9$ V f = 4.4 MHz V_i = 400 mV		900		Ω
$\|Z_8\|$	Parallel input impedance at pin 8			900		Ω

NOTES: * Adjustable to the same level of V_7 by variable resistors, or by variable voltages $\leqslant$ 1.2 V, connected between pins 11 and 16 for V_4 and between pins 12 and 16 for V_5.

** Maximum permissible range : 0.5 to 2 V (peak to peak).

*** Peak to peak output voltage to peak to peak input voltage ratio.

Fig. 1 - Schematic diagram

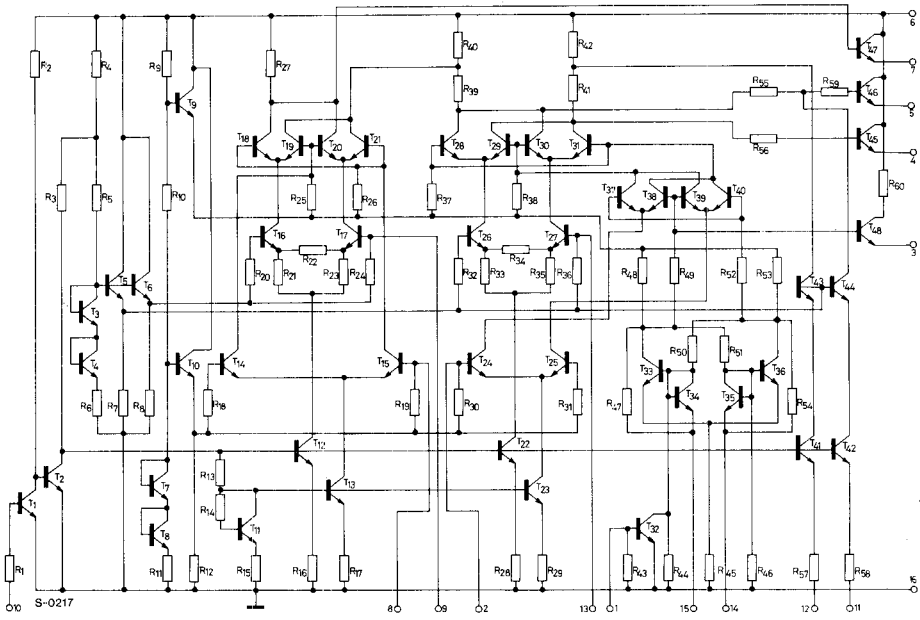


Fig. 2 - Power rating chart

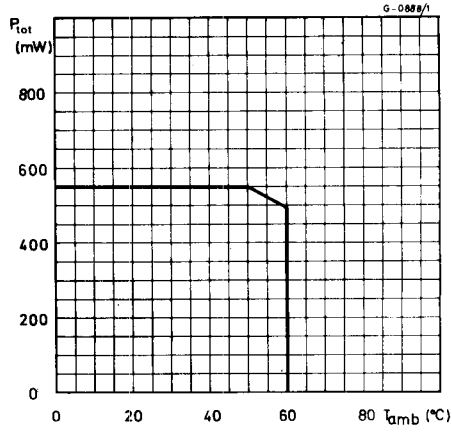


Fig. 3 - Test circuit

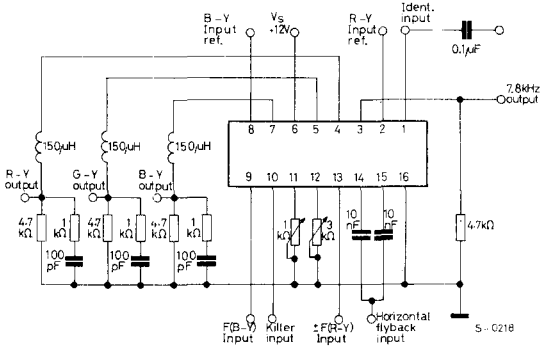


Fig. 4 - Typical application circuit