

TA8115N/F

TENTATIVE

DUAL PRE-AMPLIFIERS + HEADPHONE DRIVERS
FOR AUTOREVERSE SYSTEM IC (3V USE)

The TA8115N/F are developed for auto reverse play back headphone cassette play (3V use).

The pre-amplifiers are independent of the headphone drivers, the voltage gains of which are fixed at 27dB(Typ.).

- Switchover between Forward/Reverse input mode is possible with only one-make switch.
- Built-in Metal/Normal equalizer drivers, switchover between Metal/Normal equalizer mode is possible with only one-make switch. Those drivers are applicable to LED driver for Forward/Reverse directional display, too.
- Operating supply voltage range.

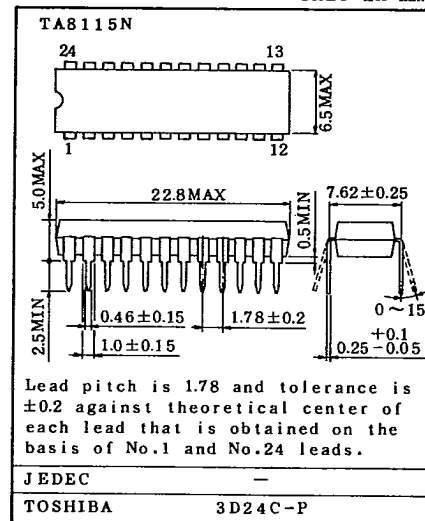
$$V_{CC}(\text{opr}) = 1.8 \sim 6V \quad (T_a = 25^\circ\text{C})$$

MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		VCC	6	V
Power Dissipation (Note)	TA8115N	P _D	1200	mW
	TA8115F		400	
Operating Temperature		T _{opr}	-25~75	°C
Storage Temperature		T _{stg}	-55~150	°C

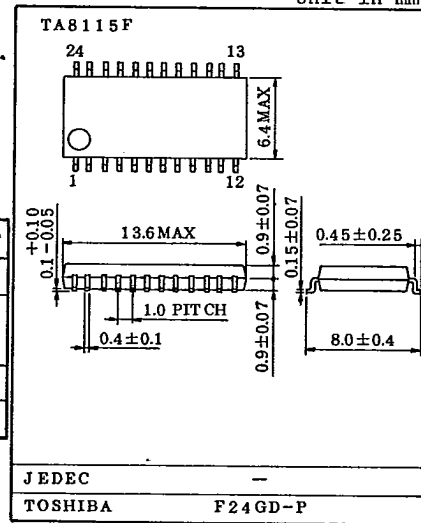
Note: Derated above $T_a = 25^\circ\text{C}$ in the proportion of 9.6mW/°C for TA8115N, and of 3.2mW/°C for TA8115F.

Unit in mm



Weight : 1.2g

Unit in mm



Weight : 0.31g

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TA8115N/F

ELECTRICAL CHARACTERISTICS

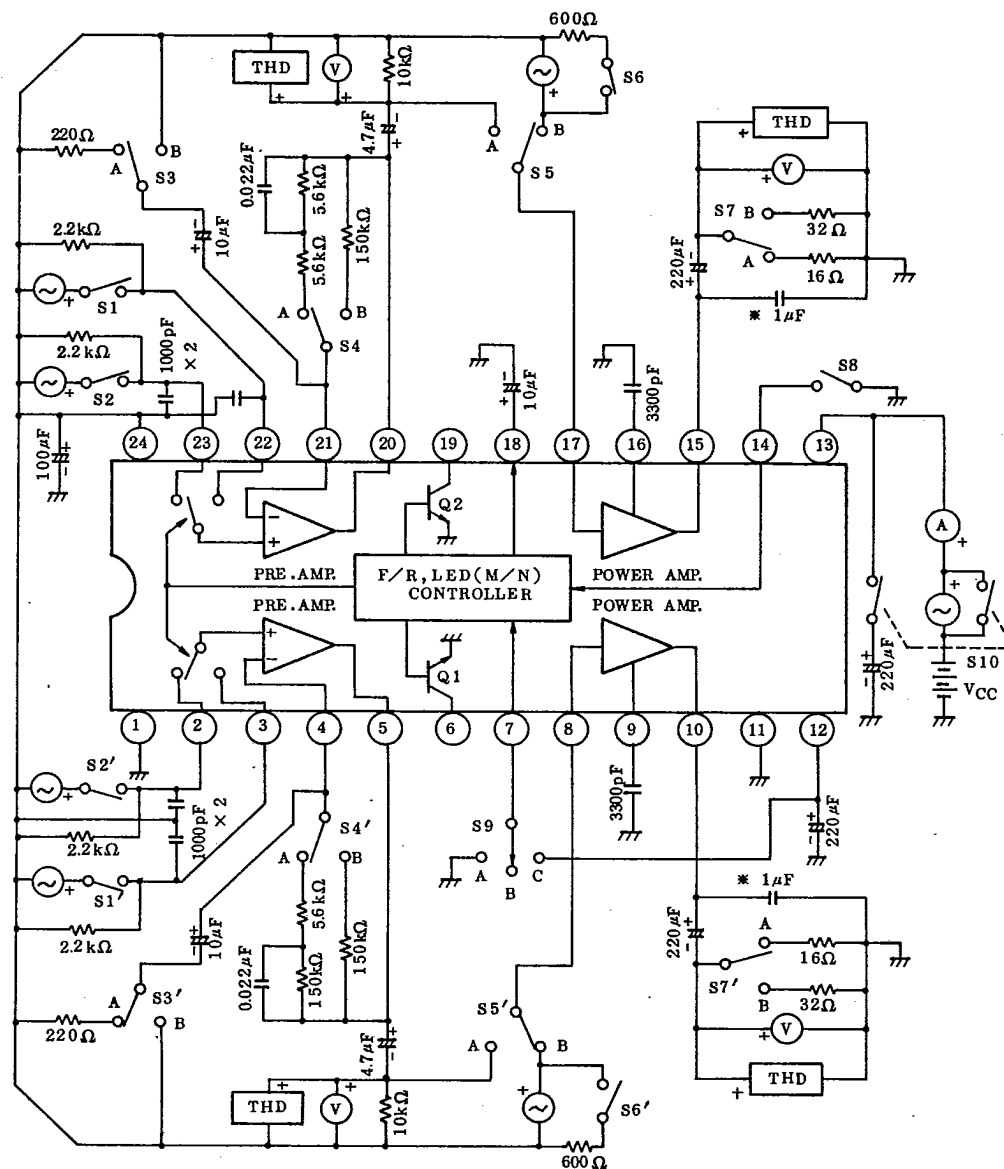
(Unless otherwise specified. $V_{CC}=3V$, $f=1kHz$, $R_L=16\Omega$, $T_a=25^\circ C$)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current		ICCQ	1	$V_{IN}=0$	-	9	16	mA
Pre-Amplifier Section	Open Loop Voltage Gain	GVO	1	$V_{OUT}=-10dBm$	68	80	-	dB
	Maximum Output Voltage	VOM	1	THD=1%	300	450	-	mVrms
	Total Harmonic Distortion	THD1	1	$V_{OUT}=-10dBm$	-	0.02	0.1	%
	Equivalent Input Noise Voltage	VNI	1	$R_g=2.2k\Omega$ $BW=20Hz\sim 20kHz$ $NAB(G_v=33dB, f=1kHz)$	-	0.9	1.5	μV_{rms}
	Ripple Rejection Ratio	RR1	1	$V_{rip}=-10dBm$ $f=100Hz, R_g=2.2k\Omega$	45	60	-	dB
	Input Bias Current	IB1	3	$V_{IN}=0$	-	0.5	1.5	μA
	Cross Talk (Forward/Reverse)	CTFR	1	$V_{OUT}=-10dBm$ $R_g=2.2k\Omega$ $BW=20Hz\sim 20kHz$	63	73	-	dB
Headphone Driver Section	Output Power	POUT	1	THD=10%, $R_L=16\Omega$	38	50	-	mW
	Closed Loop Voltage Gain	GVC	1	$V_{OUT}=-10dBm$	25	27	29	dB
	Total Harmonic Distortion	THD2	1	$POUT=1mW$	-	0.3	2.0	%
	Output Noise Voltage	VNO	1	$R_g=600\Omega$ $BW=20Hz\sim 20kHz$	-	25	70	mVrms
	Ripple Rejection Ratio	RR2	1	$V_{rip}=-10dBm$ $f=100Hz, R_g=600\Omega$	45	60	-	dB
	Input Resistance	RIN	1	-	-	20	-	$k\Omega$
	Input Bias Current	IB2	3	$V_{IN}=0, R_g=100k\Omega$	-	5	40	nA
	Channel Balance	CB	1	$V_{OUT}=-10dBm$	-	-	1	dB
	ON-Resistance of Metal Driver	RON	2	-	-	20	-	Ω
	Maximum LED Current	I _{LED}	4	$V_{CE}=0.3V$	3.5	-	-	mA
Pre + Driver	Cross Talk (L/R)	CTLR	1	$V_{OUT}=-5dBm$ (Driver) $BW=20Hz\sim 20kHz$	40	53	-	dB
	Signal Leakage	SL	1	$V_{OUT}=12dBm$ (Pre) $BW=20Hz\sim 20kHz$	55	63	-	dB

AUDIO LINEAR IC

TA8115N/F

TEST CIRCUIT 1



*: Monolithic ceramic condenser

* See the "switch state for electrical characteristics".

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SWITCH STAGE FOR ELECTRICAL CHARACTERISTICS

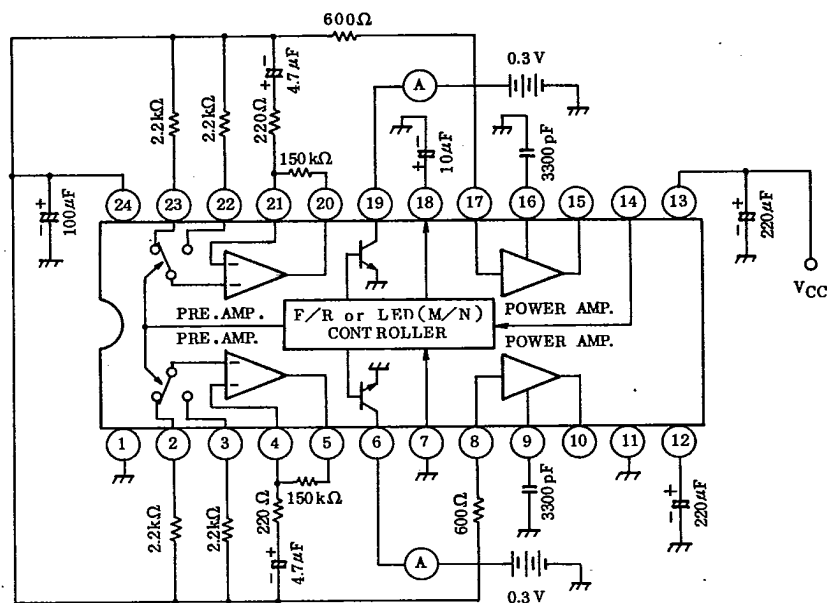
x OFF, O ON

SW Character- istic	S1	S1'	S2	S2'	S3	S3'	S4	S4'	S5	S5'	S6	S6'	S7	S7'	S8	S9	S11
ICCQ	x	x	x	x	A	A	A	A	B	B	O	O	A	A	x	B	O
GVO	O	O	O	O	B	B	B	B	B	B	O	O	A	A	O/x	B	O
THD1	O	O	O	O	A	A	A	A	B	B	O	O	A	A	O/x	B	O
VOM	O	O	O	O	A	A	A	A	B	B	O	O	A	A	O/x	B	O
VNI	x	x	x	x	A	A	A	A	B	B	O	O	A	A	O/x	B	O
CTFR	O/x	O/x	x/O	x/O	A	A	A	A	B	B	O	O	A	A	x+O	B	O
POUT	x	x	x	x	A	A	A	A	B	B	x	x	A	A	x	B	O
GVC	x	x	x	x	A	A	A	A	B	B	x	x	A	A	x	B	O
THD2	x	x	x	x	A	A	A	A	B	B	x	x	A	A	x	B	O
VNO	x	x	x	x	A	A	A	A	B	B	O	O	A	A	x	B	O
CB	x	x	x	x	A	A	A	A	B	B	x	x	A	A	x	B	O
CTLR	O/x	x/O	O/x	x/O	A	A	A	A	A	A	x	x	A	A	x	B	O
SL	O	O	O	O	A	A	A	A	A	A	x	x	A	A	x	B	O
RR1	x	x	x	x	A	A	A	A	B	B	O	O	A	A	x	B	x
RR2	x	x	x	x	A	A	A	A	B	B	O	O	A	A	x	B	x

AUDIO LINEAR IC

TA8115N/F

TEST CIRCUIT 4



FUNCTION MODE TABLE (See "TEST CIRCUIT-1")

This IC is set to the mode shown in the table below, by the state of the control terminals, pin 7, pin 14.

S9	S8	Q1	Q2	PRE AMPLIFIER INPUT TERMINAL	APPLICABLE FUNCTION
C	OFF	OFF	ON	Pin 2, Pin 23	Tape Directional Display
C	ON	ON	OFF	Pin 3, Pin 22	
B	OFF	OFF	OFF	Pin 2, Pin 23	EQ ; Normal
B	ON	OFF	OFF	Pin 3, Pin 22	
A	OFF	ON	ON	Pin 2, Pin 23	EQ : Metal
A	ON	ON	ON	Pin 3, Pin 22	

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TA8115N/F**DC CHARACTERISTICS**

(VCC=3V, VIN=0, RL=16Ω, Ta=25°C, TEST CIRCUIT-5)

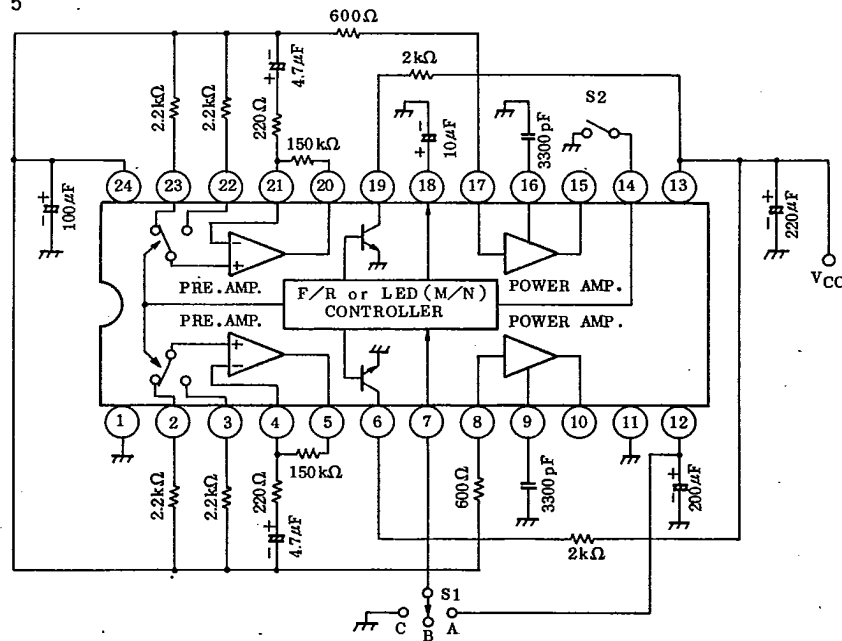
(Unit : V)

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
Terminal Voltage	0	1.5	1.5	1.5	1.5	Note	Note	1.5	0.7	1.5	0	2.6

TERMINAL No.	13	14	15	16	17	18	19	20	21	22	23	24
Terminal Voltage	3.0	Note	1.5	0.7	1.5	Note	Note	1.5	1.5	1.5	1.5	1.5

Note: These terminals are set to the voltages shown in the table below, by the control switches S1, S2.

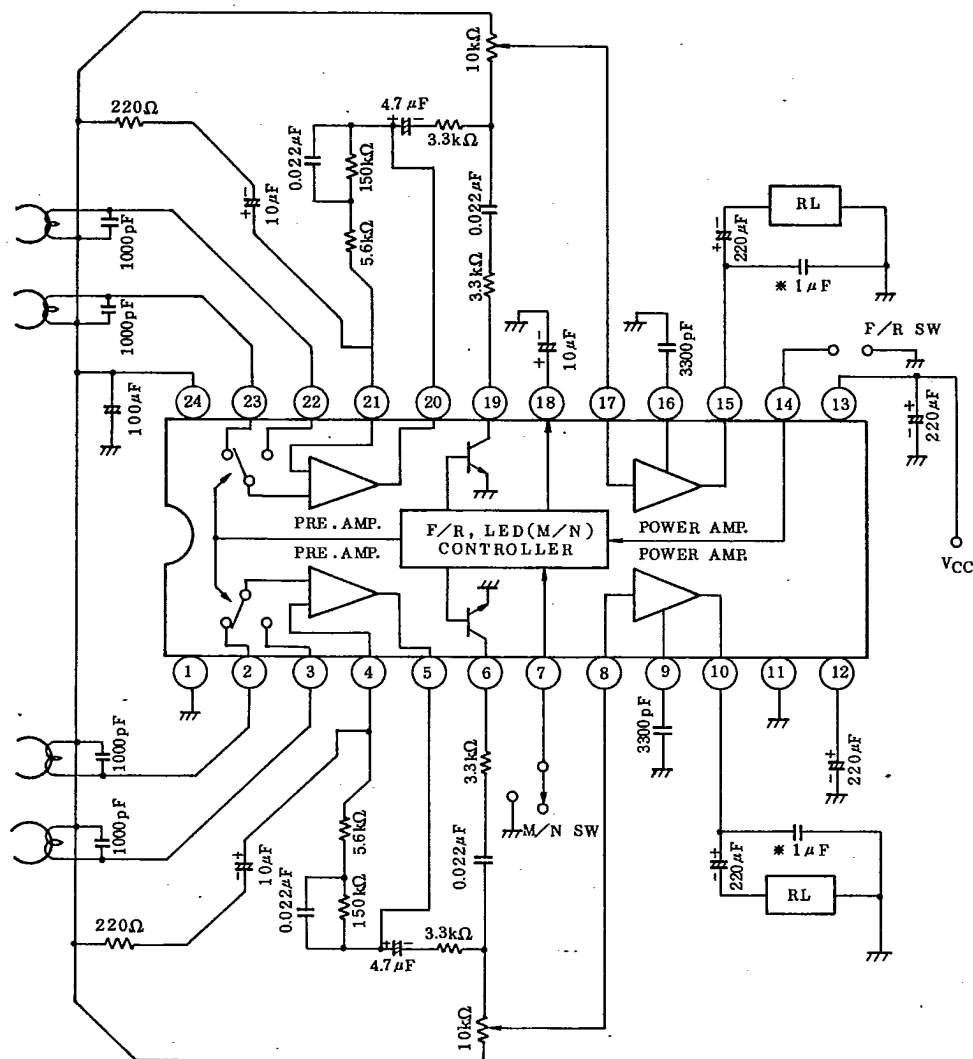
SWITCH MODE		TERMINAL VOLTAGE (V)				
S1	S2	Pin 6	Pin 7	Pin 14	Pin 18	Pin 19
A	OFF	3.0	2.6	0.6	0	<0.3
	ON	<0.3	2.6	0	0.6	3.0
B	OFF	3.0	0.2	0.6	0	3.0
	ON	3.0	0.2	0	0.6	3.0
C	OFF	<0.3	0	0.6	0	<0.3
	ON	<0.3	0	0	0.6	<0.3

TEST CIRCUIT 5**TOSHIBA**

T-77-21

TA8115N/F

APPLICATION CIRCUIT 2 (Equalizer switchover between Normal/Metal mode)



* : Monolithic ceramic condenser

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TA8115N/F

APPLICATION NOTE FOR PATTERN LAYOUT

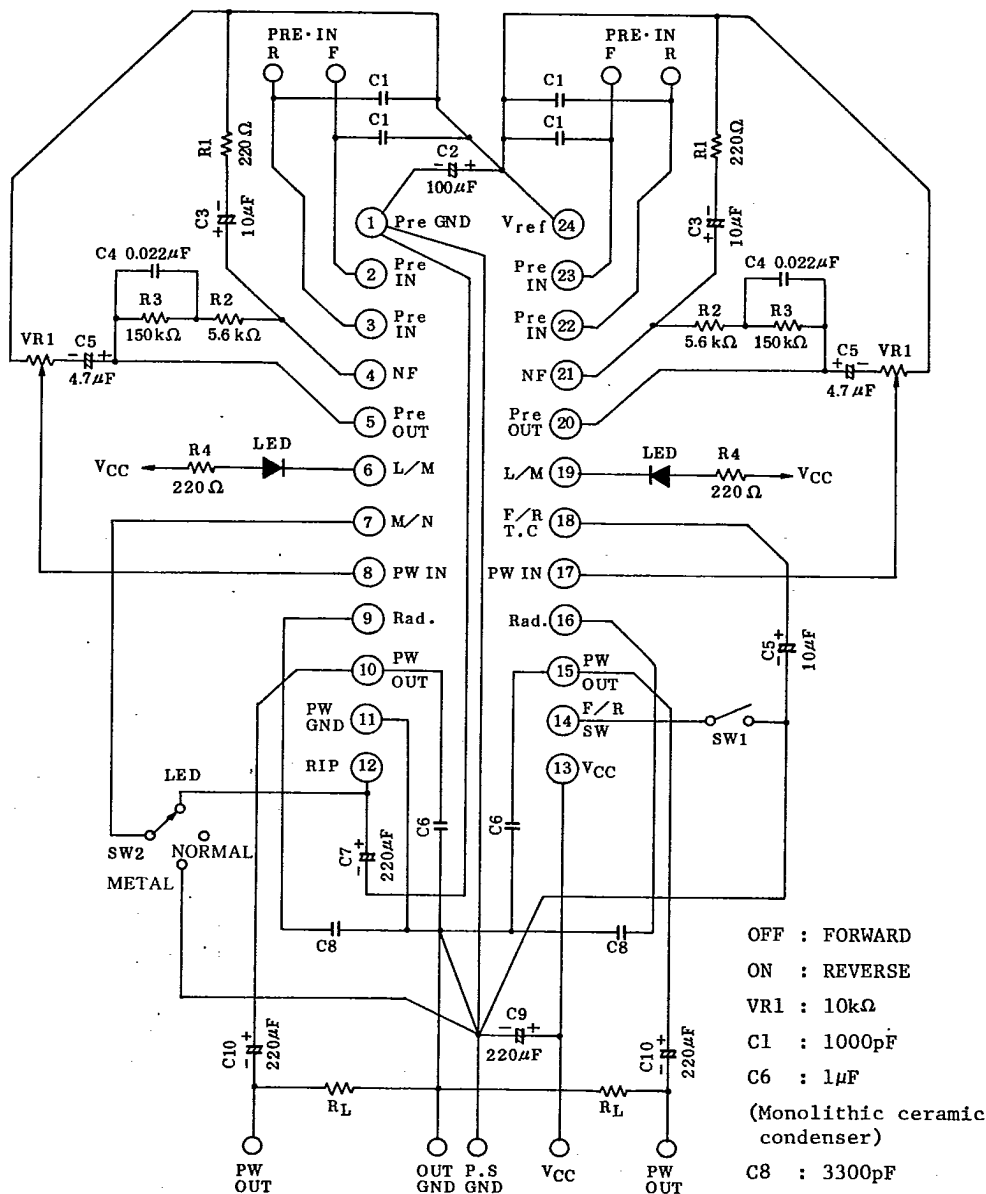
- (1) The GND line of pin 1 (Pre GND) must be isolated from that of pin 11 (PW GND) at the GND point, where the V_{CC} decoupling condenser C9 is placed.
- (2) The GND line of C1 (for Ripple Filter) must be isolated from that of condenser C2 (for Reference Voltage), at the point of pin 1.
- (3) The pattern diagram between the pin 24 (terminal of V_{REF}) and the condenser C2 must be made shortly. As for the pin 1 (Pre GND), it's as well.
- (4) The pattern diagram between the pin 11 (PW GND) and the compensation condenser, C6 must be shortly. And this positive line of C6 must be kept away from the terminals of PW IN, pin 8, 17.
- (5) The lines of PW IN must be kept away from those of PW OUT. And each of the PW OUT lines must be kept away.
- (6) The line of PW GND (pin 11) must be isolated from the load GND lines, at the GND point, where the V_{CC} decoupling condenser C9.
- (7) The GND lines of condensers C8, which are for compensation of radiation, must be isolated from other GND lines to pin 11.

* See the example of pattern layout as shown next page.

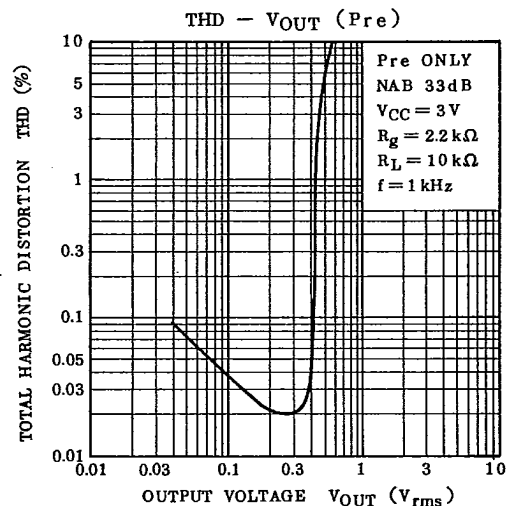
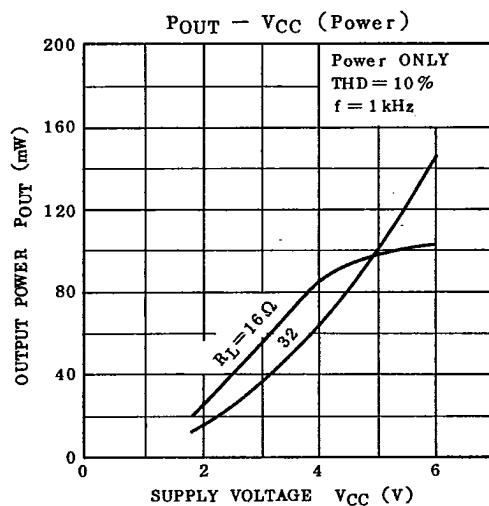
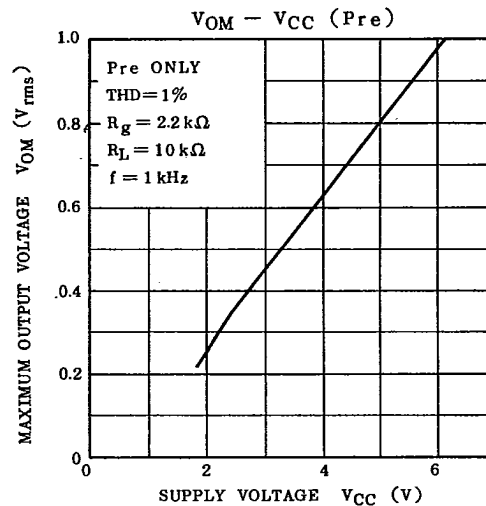
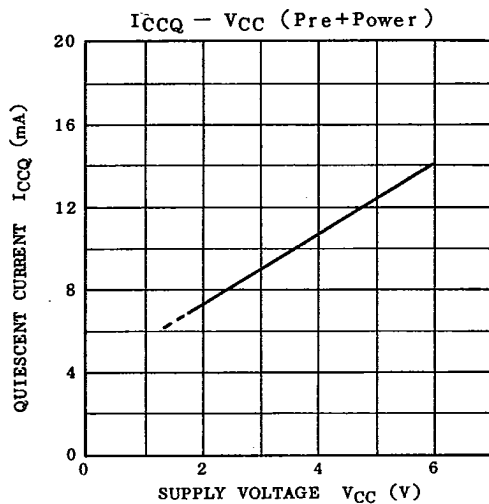
AUDIO LINEAR IC

TA8115N/F

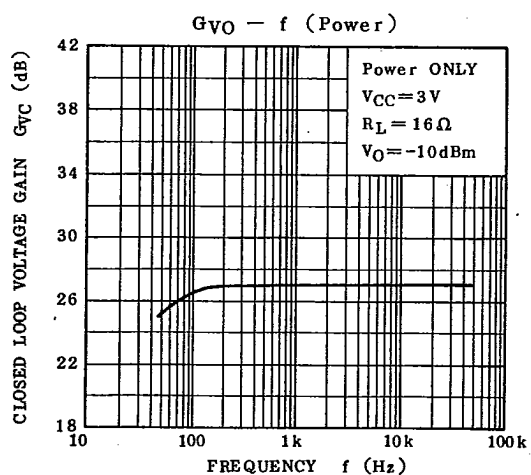
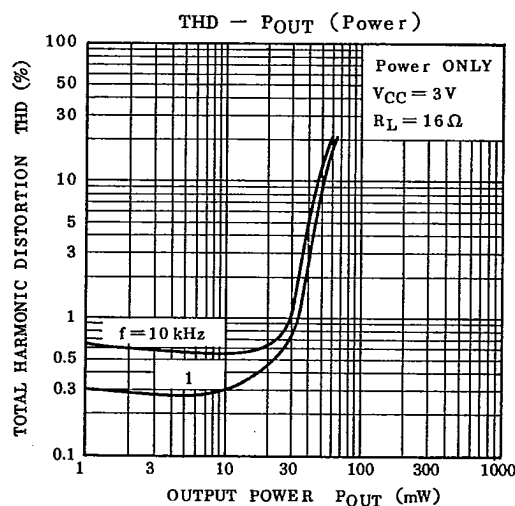
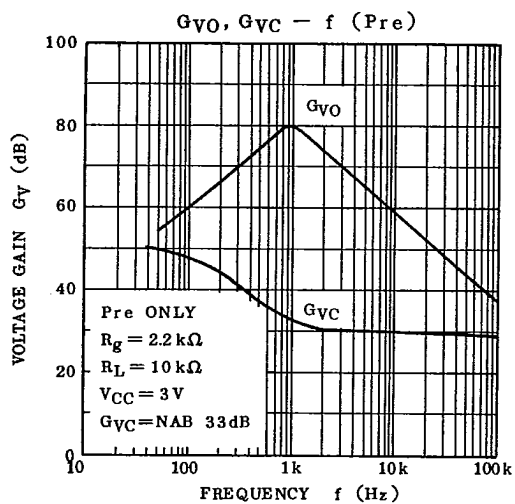
AN INSTANCE FOR RECOMMENDED PCB PATTERN LAYOUT

**TOSHIBA**

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