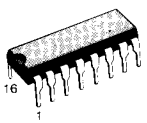
T54LS75
T74LS75

PRELIMINARY DATA

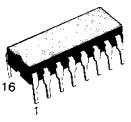
4-BIT D LATCH

DESCRIPTION

The T54LS/T74LS75 is a 4-bit D latch; it is applied as temporary storage for binary information between processing units and input/output or indicator units. When the Enable is HIGH, the information present at a data (D) input shifts to the Q output, which follows the data input on condition that the Enable remains HIGH. If the Enable goes LOW, the information is kept at the Q output until the Enable is allowed to go HIGH.



B1
Plastic Package



D1/D2
Ceramic Package

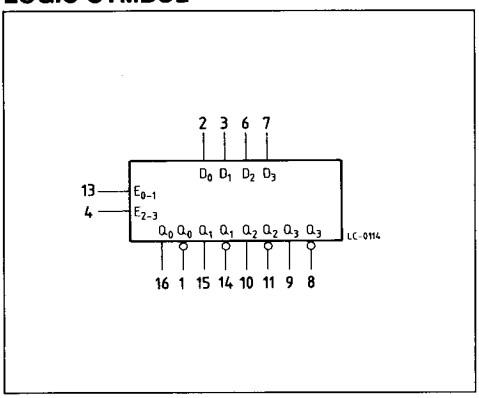
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

T54LS75 D2	T74LS75 C1
T74LS75 D1	T74LS75 M1
T74LS75 B1	

LOGIC SYMBOL



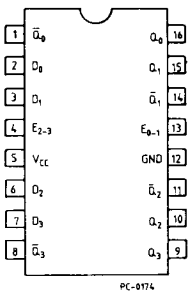
V_{CC} = Pin 5
GND = Pin 12

PIN NAMES

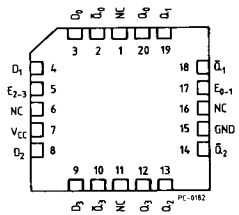
D_1-D_4	Data Inputs
E_{0-1}	Enable Input Latches 0, 1
E_{2-3}	Enable Input Latches 2, 3
Q_1-Q_4	Latch Outputs
$\overline{Q}_1$-$\overline{Q}_4$	Complementary Latch Outputs

PIN CONNECTION
(top view)

DUAL IN LINE

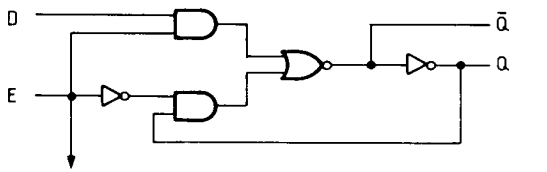


CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM AND TRUTH TABLE



(Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

Notes:

t_n = bit time before clock negative-going transition

t_{n+1} = bit time after clock negative-going transition

V_{CC} = Pin 5
GND = Pin 12
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS75D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS75XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.5			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	
I_{IH}	Input HIGH Current	D Input			20	V_{CC} = MAX, V_{IN} = 2.7V	μA
		E Input			80		
		D Input			0.1	V_{CC} = MAX, V_{IN} = 7.0V	mA
		E Input			0.4		
I_{IL}	Input LOW Current	D Input			−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
		E Input			−1.6		
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX	mA
I_{CC}	Power Supply Current				12	V_{CC} = MAX	mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions	Units
t_{PLH} t_{PHL}	Propagation Delay, Data to Q		15 9.0	27 17	V_{CC} = 5.0V C_L = 15pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Q}$		12 7.0	20 15		ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q		15 14	27 25		ns
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Q}$		16 7.0	30 15		ns

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions*	Units
		Min.	Typ.	Max.		
t_W	Enable Pulse Width	20			$V_{CC} = 5.0V$	ns
t_s	Set-up Time	20				ns
t_h	Hold Time	5				ns

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS