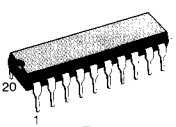
T54LS398/399
T74LS398/399

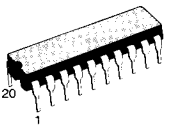
QUAD 2-PORT REGISTER

DESCRIPTION

The T54LS/T74LS398/399 are Quad 2-Port Registers. They are the logical equivalent of a quad 2-input multiplexer followed by a 4-bit edge-triggered register. Selection between two 4-bit input ports (data soutces). The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input. The T54LS/T74LS398 is composed of both Q and $\overline{Q}$ inputs, while the T54LS/T74LS399 features only Q inputs.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

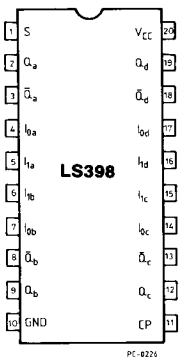
ORDERING NUMBERS:

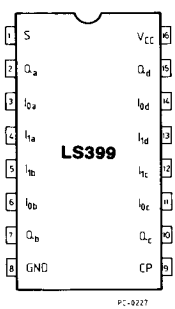
T54LSXXX D2	T74LSXXX C1
T74LSXXX D1	T74LSXXX M1
T74LSXXX B1	

- FULLY POSITIVE EDGE-TRIGGERED OPERATION
- BOTH TRUE AND COMPLEMENTED OUTPUTS ON T54LS/T74LS398
- SELECT FROM TWO DATA SOURCES
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- LS398 PRELIMINARY DATA

PIN CONNECTION
(top view)

DUAL IN LINE



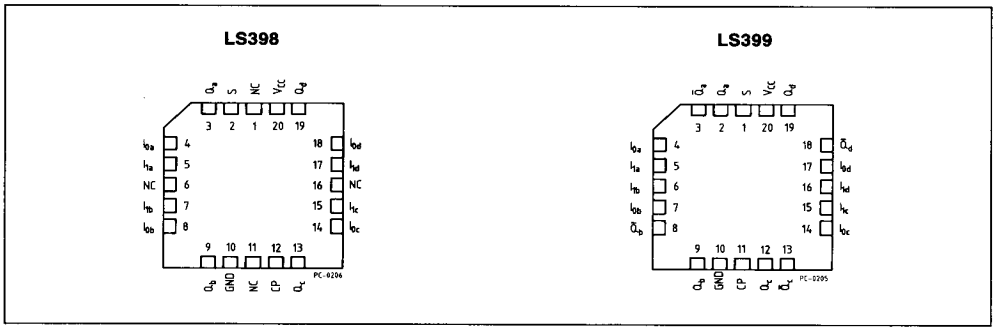


NC = No Internal Connection

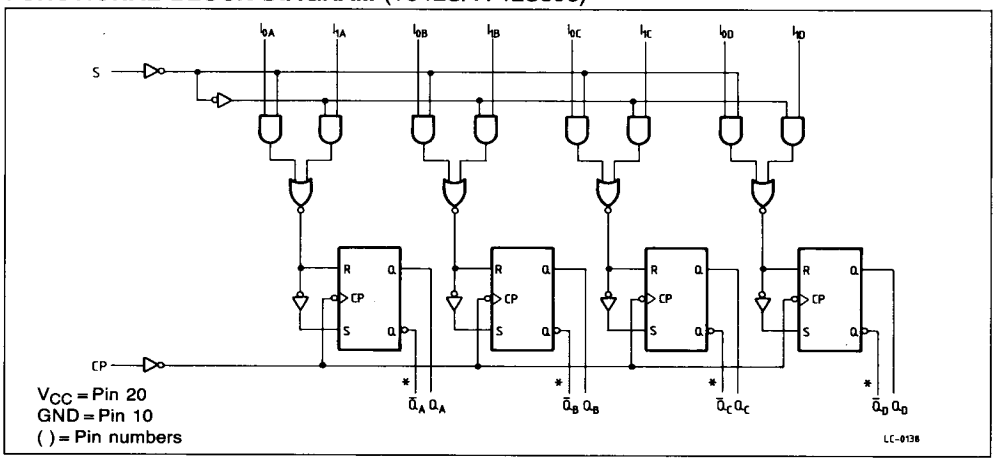
PIN NAMES

S	Common Selct Input
CP	Clock (Active HIGH going edge) Input
I_{0a}-I_{0d}	Data Input From Source 0
I_{1a}-I_{1d}	Data Input From Source 1
Q_a-Q_d	Register True Outputs
Q_a-Q_d	Register Complementary Outputs

CHIP CARRIER



FUNCTIONAL BLOCK DIAGRAM (T54LS/T74LS398)



FUNCTIONAL DESCRIPTION

These high speed Quad 2-Port Registers select four bits of data from two sources (Port) under the control of a Common Select Input (S). The 4-bit Output Register where selected data are transferred is synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit RS type output register is fully edge-triggered. Predictable operation is assured if Data inputs (I) and select inputs (S) are kept stable only a set-up time prior to and hold time after the LOW-to-HIGH transition of the Clock input. Both and $\overline{Q}$ inputs are available in the LS398.

TRUTH TABLE

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

* T54LS/T74LS398 only
L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS398/399D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS398/399XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units
			Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V_{CC} = MIN, I_{OH} = −400mA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.5			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA	
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CC}	Power Supply Current				13	V_{CC} = MAX	mA

AC CHARACTERISTICS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output Q		18 21	27 32	V_{CC} = 5.0V C_L = 15pF	ns

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_W	Clock Pulse Width	20			V_{CC} = 5.0V	ns
t_s	Data Set-up Time	25				ns
t_s	Select Set-up Time	45				ns
t_h	Hold Time, Any Input	0				ns

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

Fig. 1

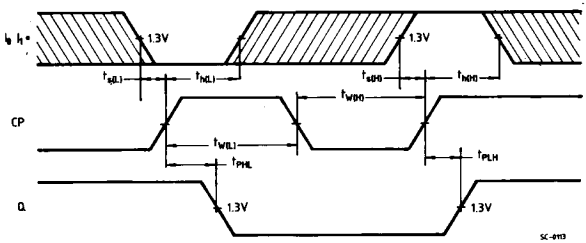


Fig. 2

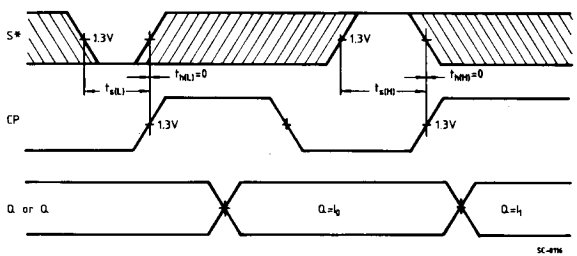
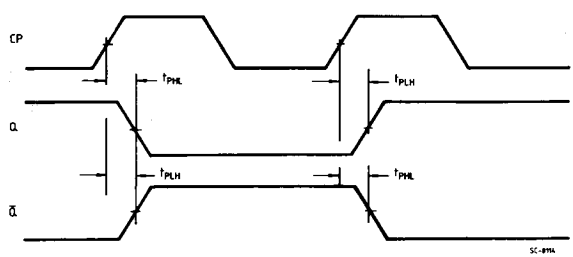


Fig. 3



* The shaded areas indicate when the input is permitted to change for predictable output performance.