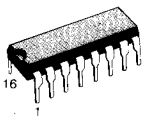
T54LS298
T74LS298

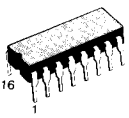
QUAD 2-PORT REGISTER (QUAD 2-INPUT MULTIPLEXER WITH STORAGE)

DESCRIPTION

The T54LS298/T74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronously with the HIGH to LOW transition of the Clock input. The LS298 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all SGS TTL families.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

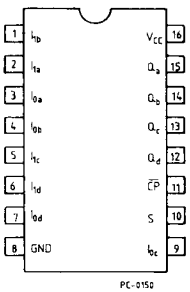
ORDERING NUMBERS:

T54LS298 D2	T74LS298 C1
T74LS298 D1	T74LS298 M1
T74LS298 B1	

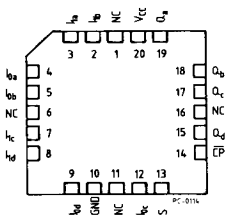
- SELECT FROM TWO DATA SOURCES
- FULLY EDGE-TRIGGERED OPERATION
- TYPICAL POWER DISSIPATION OF 65mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

PIN NAMES

S	Common Select Input
$\overline{CP}$	Clock (Active LOW Going Edge) Input
I_{0a}-I_{0b}	Data Inputs From Sources 0
I_{1a}-I_{1b}	Data Inputs From Sources 1
Q_a-Q_b	Register Outputs

TRUTH TABLE

INPUTS			OUTPUT
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

_ = LOW Voltage Level
¯ = HIGH Voltage Level
x = Don't Care
= LOW voltage level one set-up time prior to the LOW to HIGH clock transition
= HIGH voltage level one set-up time prior to the LOW to HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

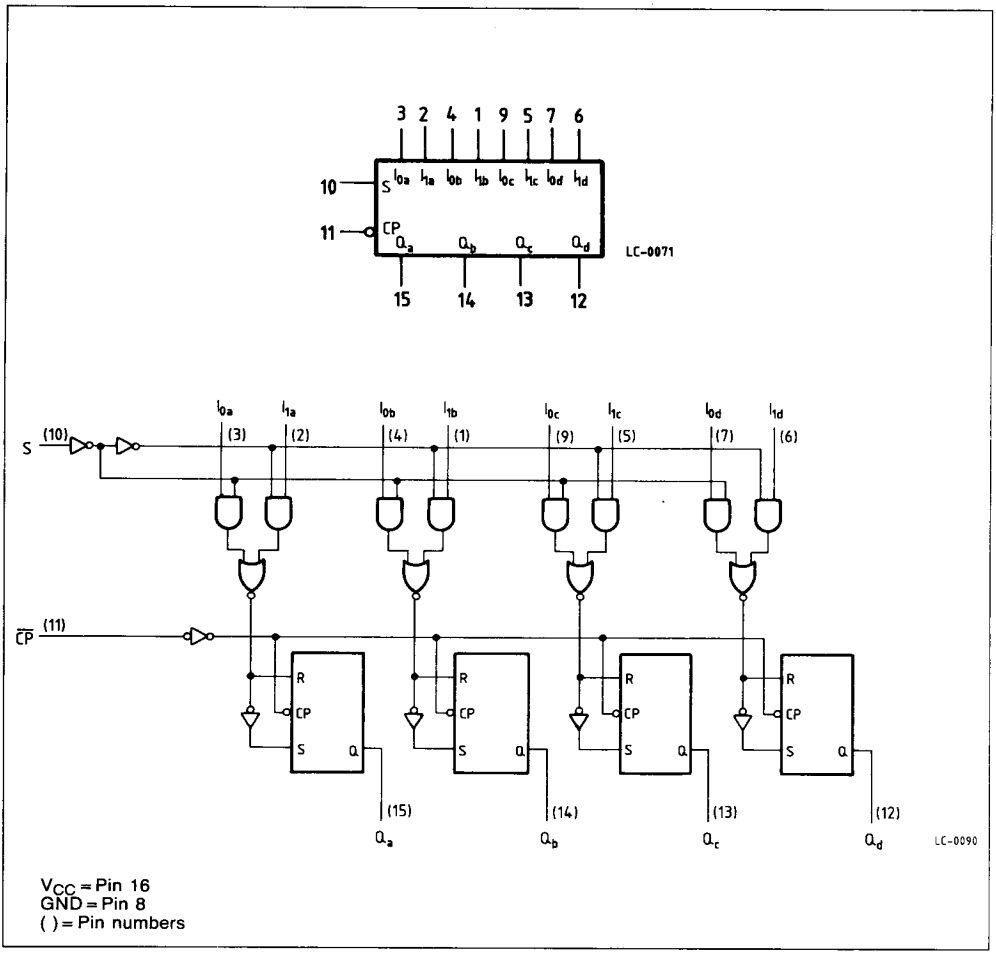
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS298D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS298XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

LOGIC SYMBOL AND LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input (CP). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one set-up time prior to the HIGH to LOW transition of the clock for predctable operation.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)		Units
			Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Threshold Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Threshold Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table		V
		74	2.7	3.4				
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V		μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current			13	21	V_{CC} = MAX		mA

AC CHARACTERISTICS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH}	Propagation Delay, Clock to Output		18	27	Fig. 1	V_{CC} = 5.0V C_L = 15pF	ns
t_{PHL}	Propagation Delay, Clock to Output		21	32	Fig. 1		ns

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
$t_{W(H)}$	Clock Pulse Width (HIGH)	20	11		Fig. 1	$V_{CC} = 5.0V$	ns
$t_{W(L)}$	Clock Pulse Width (LOW) (HIGH or LOW)	20	11				ns
$t_{s(Data)}$	Set-Up Time, Data to Clock	15	10		Fig. 1		ns
$t_{h(Data)}$	Hold Time, Data to Clock	5.0	1				ns
$t_{s(S)}$	Set-Up Time, Select to Clock	25	20		Fig. 2		ns
$t_{h(S)}$	Hold Time, Select to Clock	0	−2				ns

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

Fig. 1

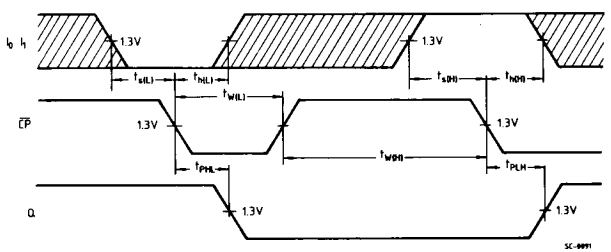
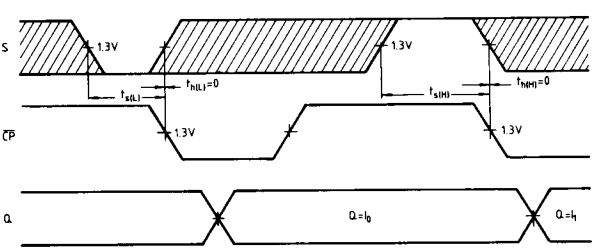


Fig. 2



* The shaded areas indicate when the input is permitted to change for predictable output performance.