



## LS290-DECADE COUNTER LS293-4-BIT BINARY COUNTER

### DESCRIPTION

The T54LS/T74LS290 and T54LS/T74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to  $\overline{CP}$ ) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

**B1**  
Plastic Package

**D1/D2**  
Ceramic Package

**M1**  
Micro Package

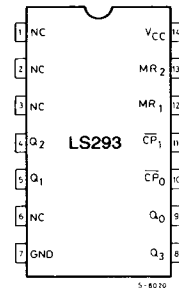
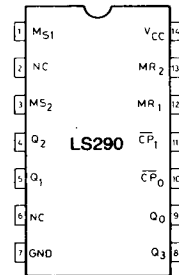
**C1**  
Plastic Chip Carrier

**ORDERING NUMBERS:**  
 T54LSXXX D2                    T74LSXXX C1  
 T74LSXXX D1                    T74LSXXX M1  
 T74LSXXX B1

- CORNER POWER PIN VERSION OF THE LS90 AND LS93
- LOW POWER CONSUMPTION... TYPICALLY 45mW
- HIGH COUNT RATES... TYPICALLY 50MHz
- CHOICE OF COUNTING MODES... BCD, BI-QUINARY, BINARY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

### PIN CONNECTION (top view)

#### DUAL IN LINE

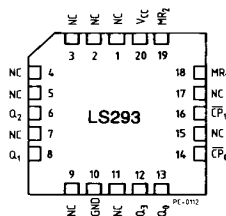
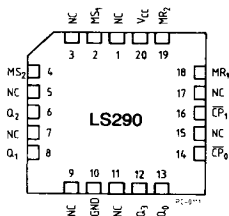


### PIN NAMES

$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to ÷ 2 Section
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to ÷ 5 Section (LS290)
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to ÷ 8 Section (LS293)
MR <sub>1</sub> , MR <sub>2</sub>	Master Reset (Clear) Inputs
MR <sub>1</sub> , MR <sub>2</sub>	Master Reset (Preset-9 LS290) Inputs
Q <sub>0</sub>	Output from - 2 Section
Q <sub>1</sub> , Q <sub>2</sub> , Q <sub>3</sub>	Outputs from - 5 & - 8 Sections



## CHIP CARRIER



NC = No Internal Connection

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to 7	V
$V_I$	Input Voltage, for $\overline{CP}$	-0.5 to 5.5	V
$V_O$	Output Voltage, Applied to Output	-0.5 to 10	V
$I_I$	Input Current, Into Inputs	-30 to 5	mA
$I_O$	Output Current, Into Outputs	50	mA

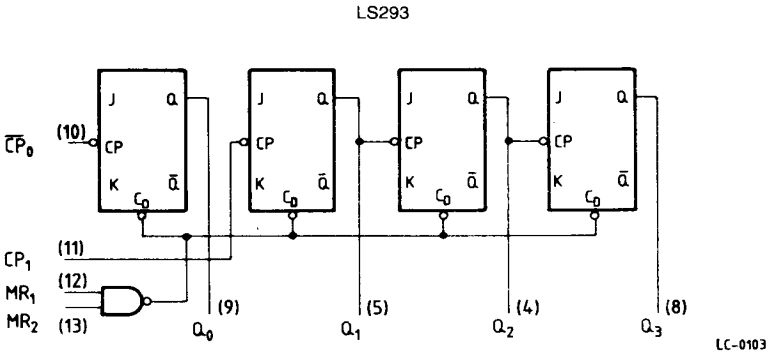
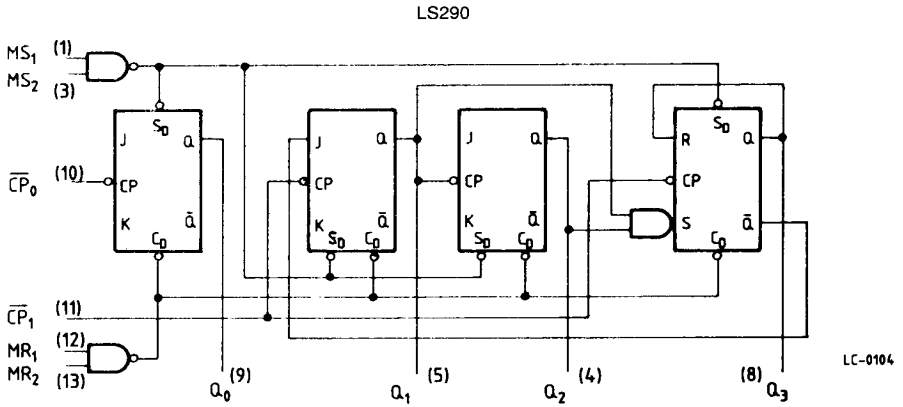
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS290/293D2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS290/293XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

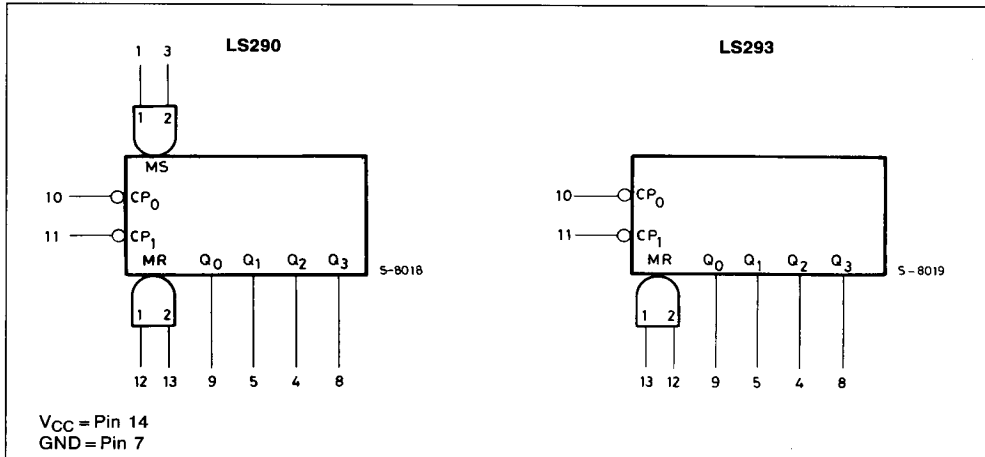
XX = package type.

**LOGIC DIAGRAMS**



V<sub>CC</sub> = Pin 14  
 GND = Pin 7  
 ( ) = Pin numbers

## LOGIC SYMBOL



## FUNCTIONAL DESCRIPTION

The LS290 and LS293 are 4-bit ripple type Decade, and 4-bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The  $Q_0$  output of each device is designed and specified to drive the rated fan-out plus the  $\overline{CP}_1$  input of the device.

A gated AND asynchronous Master Reset ( $MR_1 \cdot MR_2$ ) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous master Set ( $MS_1 \cdot MS_2$ ) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

### LS290

A. BCD Decade (8421) Counter - the  $\overline{CP}_1$  input

must be externally connected to the  $Q_0$  output. The  $\overline{CP}_0$  input receives the incoming count and BCD count sequence is produced.

- B. Symmetrical Bi-quinary Divide-By-Ten Counter - The  $Q_3$  output must be externally connected to the  $\overline{CP}_0$  input. The input count is then applied to the  $\overline{CP}_1$  input and a divide-by-ten square is obtained at output  $Q_0$ .
- C. Divide-By-Two and Divide-By-Five Counter - No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ( $\overline{CP}_0$  as the input and  $Q_0$  as the output). The  $\overline{CP}_1$  input is used to obtain binary divide-by-five operation at the  $Q_3$  output.

### LS293

- A. 4-Bit Ripple Counter - The output  $Q_0$  must be externally connected to input  $\overline{CP}_1$ . The input count pulses are applied to input  $\overline{CP}_0$ . Simultaneous division of 2, 4, 8, and 16 are performed at the  $Q_0$ ,  $Q_1$ ,  $Q_2$  and  $Q_3$  outputs as shown in the truth table.
- B. 3-Bit Ripple Counter - The input count pulses are applied to input  $\overline{CP}_1$ . Simultaneous frequency divisions of 2, 4, and 8 are available at the  $Q_0$ ,  $Q_1$ ,  $Q_2$ , and  $Q_3$  outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.



**TRUTH TABLES**

**LS290  
BCD COUNT SEQUENCE**

COUNT	OUTPUT			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q<sub>0</sub> is connected to input CP<sub>1</sub> for BCD count.

**LS290  
MODE SELECTION**

RESET/SET INPUTS				OUTPUTS			
MR <sub>1</sub>	MR <sub>2</sub>	MS <sub>1</sub>	MS <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X		Count		
X	L	X	L		Count		
L	X	X	L		Count		
X	L	L	X		Count		

**LS293  
TRUTH TABLE**

COUNT	OUTPUT			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q<sub>0</sub> is connected to input CP<sub>1</sub>.

**LS293  
MODE SELECTION**

RESET INPUTS		OUTPUTS			
MR <sub>1</sub>	MR <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
H	H	L	L	L	L
L	H		Count		
H	L		Count		
L	L		Count		

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care



### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Conditions (Note 1)		Units
		Min.	Typ.	Max.			
V <sub>IH</sub>	Input HIGH Voltage	2.0			Guaranteed input HIGH Voltage for all Inputs		V
V <sub>IL</sub>	Input LOW Voltage	54		0.7	Guaranteed input LOW Voltage for all Inputs		V
		74		0.8			
V <sub>CD</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18mA		V
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.4	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -400μA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table		V
		74	2.7	3.4			
V <sub>OL</sub>	Output LOW Voltage	54,74	0.25	0.4	I <sub>OL</sub> = 4.0mA	V <sub>CC</sub> = MIN, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	V
		74	0.35	0.5	I <sub>OL</sub> = 8.0mA		
I <sub>IH</sub>	Input HIGH Current MS, MR CP <sub>0</sub> CP <sub>1</sub> (LS290) CP <sub>1</sub> (LS293)				20 40 80 40	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7V	μA
					0.1 0.2 0.4	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 5.5V	mA
I <sub>IL</sub>	Input LOW Current MS, MR CP <sub>0</sub> CP <sub>1</sub> (LS290) CP <sub>1</sub> (LS293)				-0.4 -2.4 -3.2 -1.6	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4V	μA
I <sub>OS</sub>	Output Short Circuit Current (Note 2)	-20		-100	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0V		mA
I <sub>CC</sub>	Power Supply Current		9	15	V <sub>CC</sub> = MAX		mA

**Notes:**

- 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C

### AC SET-UP REQUIREMENTS: T<sub>A</sub> = 25°C

Symbol	Parameter	Limits				Test Conditions	Units
		LS290		LS293			
		Min.	Max.	Min.	Max.		
t <sub>w</sub>	CP <sub>0</sub> Pulse Width	15		15		Fig. 1	V <sub>CC</sub> = 5.0V
t <sub>w</sub>	CP <sub>1</sub> Pulse Width	30		30		Figs. 2,3	
t <sub>w</sub>	MS Pulse Width	15					
t <sub>w</sub>	MR Pulse Width	15		15		Fig. 2	
t <sub>rec</sub>	Recovery Time, MS to CP	25				Fig. 2,3	
t <sub>rec</sub>	Recovery Time, MR to CP	25		25		Fig. 2	

RECOVERY TIME (t<sub>rec</sub>) - is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer HIGH data to Q outputs.

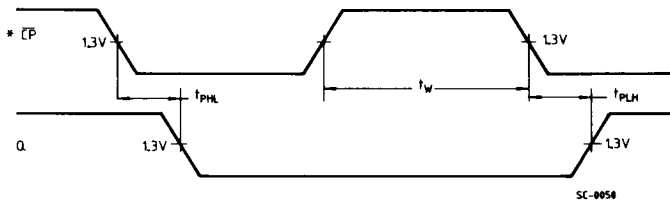


**AC CHARACTERISTICS:**  $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limits				Test Conditions		Units
		LS290		LS293				
		Min.	Max.	Min.	Max.			
$f_{MAX}$	$\overline{CP}_0$ Input Count Frequency	32		32		Fig. 1	$V_{CC} = 5.0\text{V}$ $C_L = 15\text{pF}$	MHz
$f_{MAX}$	$\overline{CP}_1$ Input Count Frequency	16		16		Fig. 1		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $\overline{CP}_0$ Input to $Q_0$ Output		16 18	16 18		Fig. 1		ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $\overline{CP}_1$ Input to $Q_1$ Output		16 21	16 21				ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $\overline{CP}_1$ Input to $Q_2$ Output		32 35	32 35				ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $\overline{CP}_1$ Input to $Q_3$ Output		32 35	51 51				ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $\overline{CP}_0$ Input to $Q_3$ Output		48 50	70 70				ns
$t_{PLH}$	MS Input to $Q_0$ and $Q_3$ Outputs		30			Fig. 3		
$t_{PHL}$	MS Input to $Q_1$ and $Q_2$ Outputs		40			Fig. 2		
$t_{PHL}$	MR Input to Any Output		40		40	Fig. 2		

**AC WAVEFORMS**

Fig. 1



\* The number of the Clock Pulse Required between the  $t_{PHL}$  and  $t_{PLH}$  measurements can be determined from the Truth Table



AC WAVEFORMS (continued)

Fig. 2

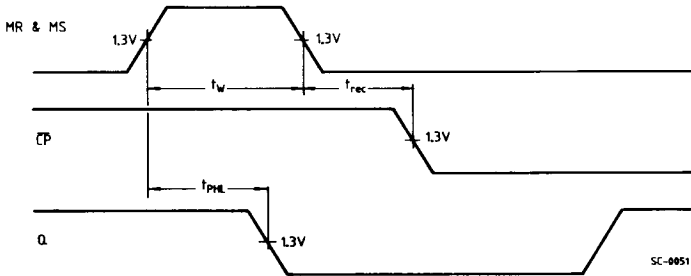


Fig. 3

