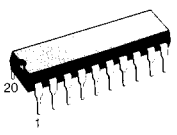
T54LS273
T74LS273

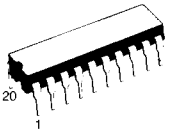
8-BIT REGISTER WITH CLEAR

DESCRIPTION

The T54LS273/T74LS273 is a high speed 8-Bit Register. The register consists of eight D-Type Flip-flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

T54LS273 D2	T74LS273 C1
T74LS273 D1	T74LS273 M1
T74LS273 B1	

- 8-BIT HIGH SPEED REGISTER
- PARALLEL REGISTER
- COMMON CLOCK AND MASTER RESET
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

TRUTH TABLE

$\overline{MR}$	CP	D_x	Q_x
L	X	X	L
H	⌐	H	H
H	⌐	L	L

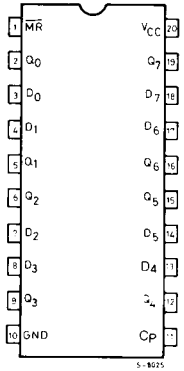
H = High Logic Level
L = Low Logic Level
X = Don't Care

PIN NAMES

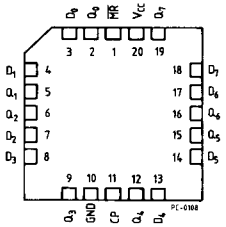
CP	Clock (Active HIGH Going Edge) Input
D_0-D_7	Data Inputs
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0-Q_7	Register Outputs

PIN CONNECTION
(top view)

DUAL IN LINE

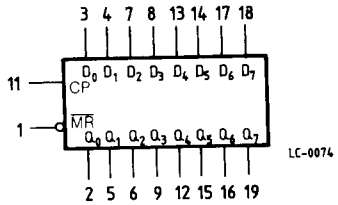


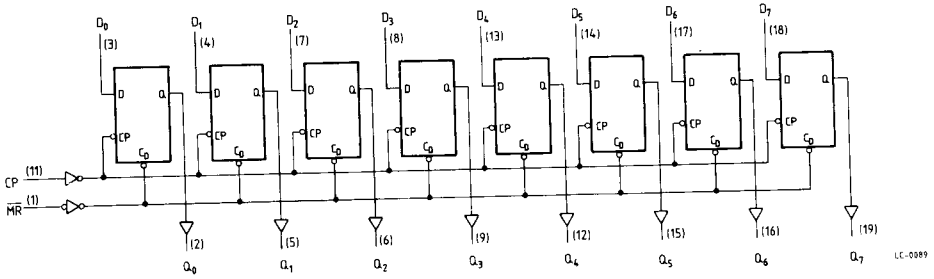
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





FUNCTIONAL DESCRIPTION

The LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.
When the MR is LOW, the Q output are LOW, independent of the other inputs. Information meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS273D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS273XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Values			Test Conditions (Note 1)	Units
			Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA	
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CC}	Supply Current			17	27	V_{CC} = MAX	mA

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		17 18	27 27	Fig. 1	$V_{CC} = 5.0V$	ns
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q Output		18	27	Fig. 1		ns
f_{MAX}	Maximum Input Clock Frequency	30	40		Fig. 2		MHz

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
$t_W(CP)$	Minimum Clock Pulse Width	20			Fig. 1	$V_{CC} = 5.0V$	ns
t_s	Set-up Time, Data to Clock (HIGH or LOW)	20			Fig. 1		ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Fig. 1		ns
t_{rec}	Recovery Time	25			Fig. 2		ns
$t_W\overline{MR}$	Minimum $\overline{MR}$ Pulse Width	20			Fig. 2		ns

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) - is defined as the minimim time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

Fig. 1 Clock to Output Delays, Clock Pulse Width, Frequency, Set-Up and Hold Times Data to Clock

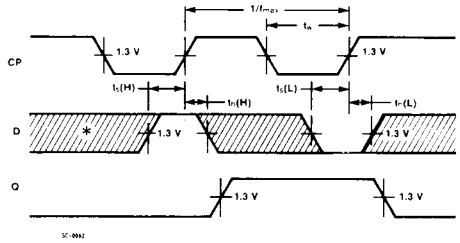
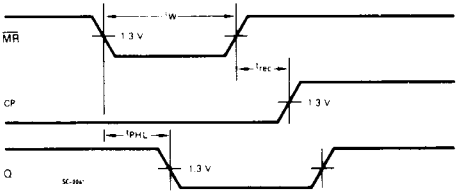


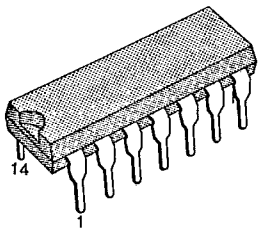
Fig. 2 Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

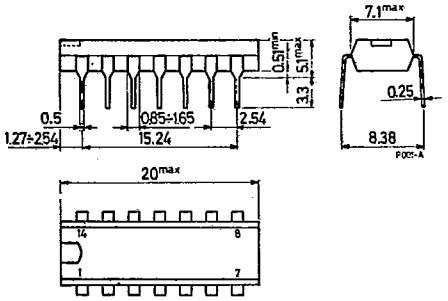


* The shaded areas indicate when the input is permitted to change for predictable output performance.

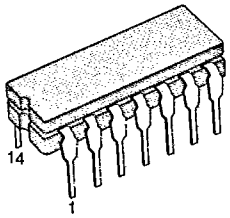
Packages

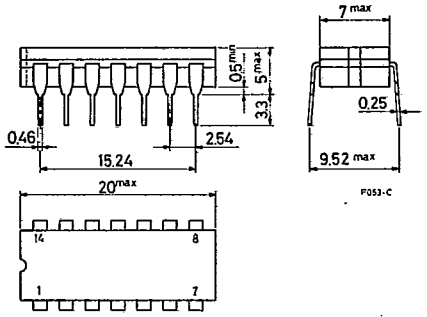
14-LEAD PLASTIC DIP





14-LEAD CERAMIC DIP





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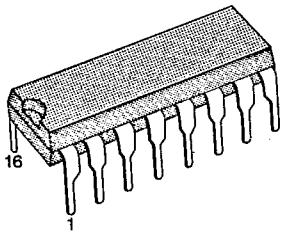
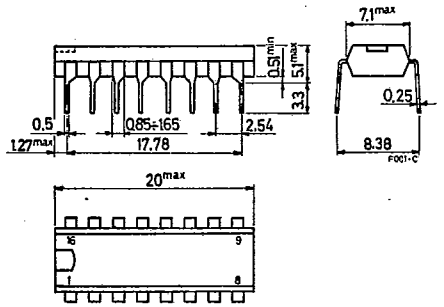
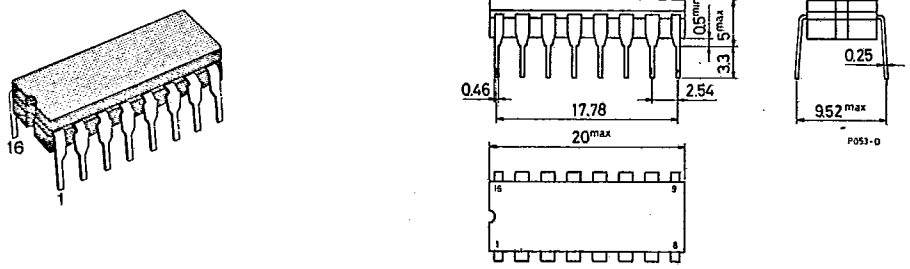




Packages

16-LEAD CERAMIC DIP



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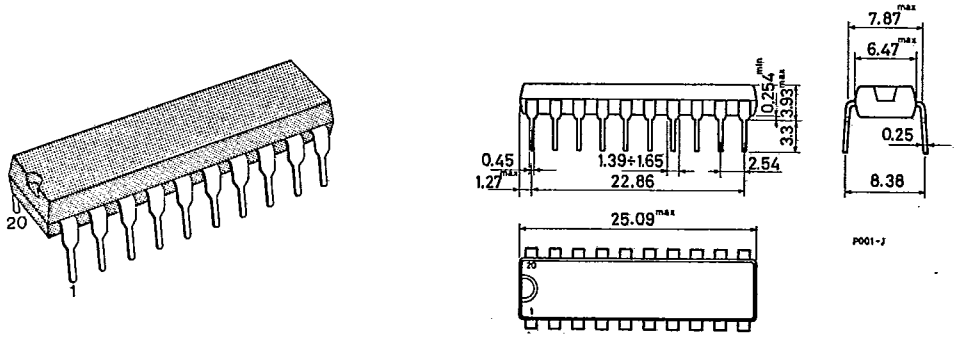
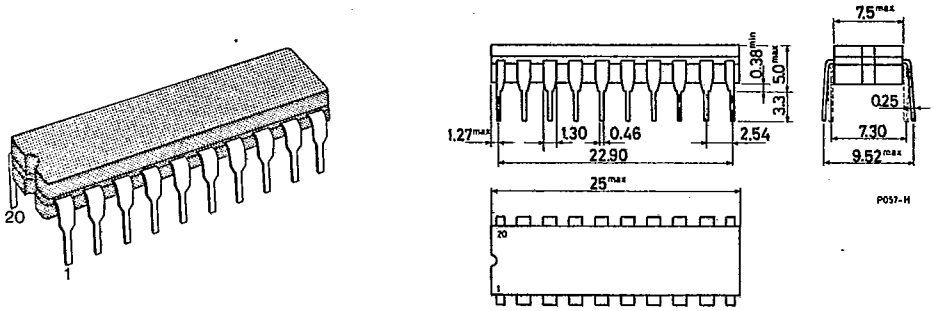
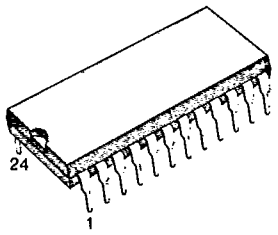


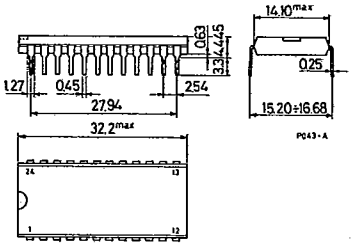
20-LEAD CERAMIC DIP



Packages

24-LEAD PLASTIC DIP





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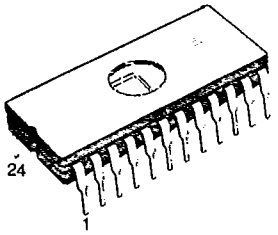
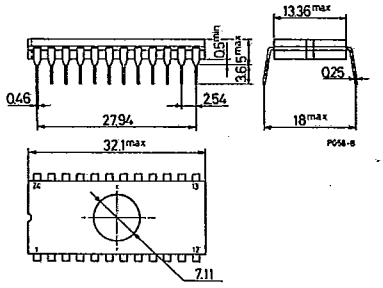
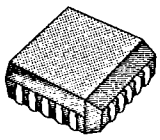
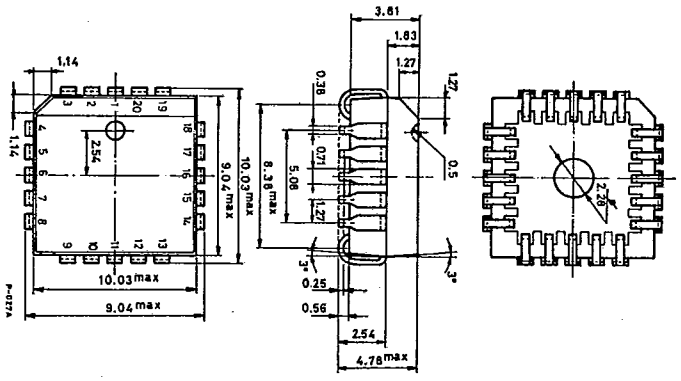




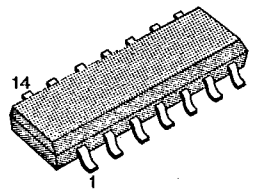
CHIP CARRIER 20 LEAD PLASTIC

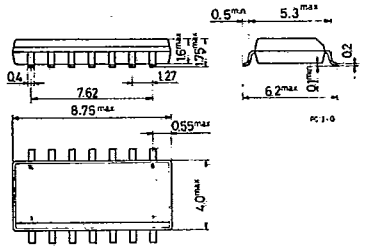




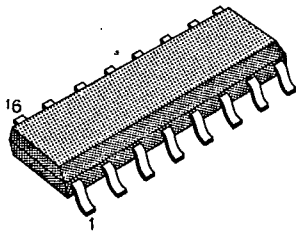
Packages

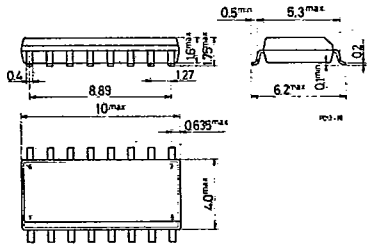
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.