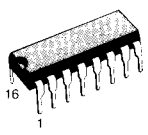
T54LS257/257A
T74LS257/257A

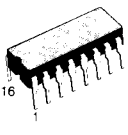
QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION

The LSTTL/MSI T54LS257/257A, T74LS257/257A is a Quad 2-Input Multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Outputs Enable ($\overline{E}_0$) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Scottky barrier diode process for high speed and is completely compatible with all SGS TTL families.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

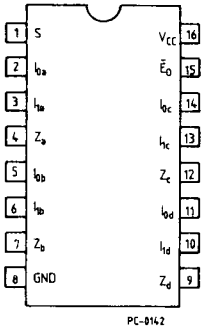
ORDERING NUMBERS:

T54LSXXX D2
T74LSXXX D1
T74LSXXX B1
T74LSXXX C1
T74LSXXX M1

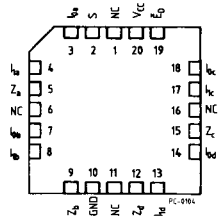
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER
- NON-INVERTING 3 STATE OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE
- VERSION "A" PRELIMINARY DATA

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER

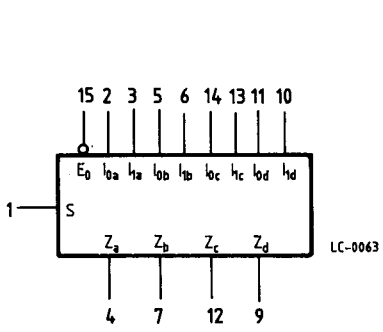


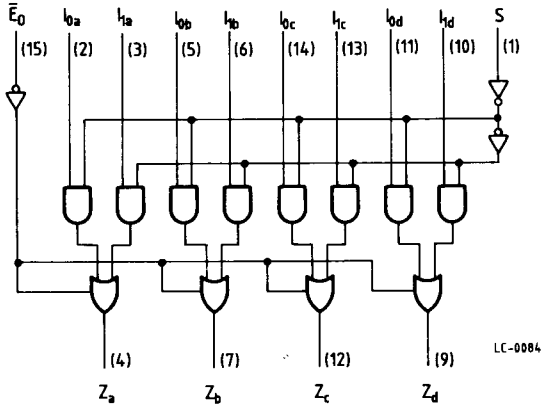
NC = No Internal Connection

PIN NAMES

S	Common Select Input
$\overline{E}_0$	Output Enable (Active LOW) Input
I_{0a}-I_{0d}	Data Inputs from Source 0
I_{1a}-I_{1d}	Data Inputs from Source 1
Z_a-Z_d	Multiplexer Output

LOGIC SYMBOL AND LOGIC DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 5.5	V
V_O	Output Voltage, Applied to Output	−0.5 to 5.5	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS257/257AD2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS257/257AXX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS257/257A is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select Input. When the Select Input is LOW, the I_0 inputs are selected and when Selected is HIGH, the I_1 inputs are selected. The data on the selected inputs appear at the outputs in true (non-inverted) form. The LS257 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The Logic equations for outputs are show below:

$$Z_a = \overline{E}_0 \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = \overline{E}_0 \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$Z_c = \overline{E}_0 \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = \overline{E}_0 \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

When the Output Enable Input ($\overline{E}_0$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers shoud ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{E}_0$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(Z) = High impedance (off)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (T54LS/T74LS257)

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units
			Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		I_{OH} = −1.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.4	3.1		I_{OH} = −2.6mA	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8mA	
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.7V, $V_{\overline{E}}$ = 2.0V	μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_{OUT} = 0.4V, $V_{\overline{E}}$ = 2.0V	μA
I_{IH}	Input HIGH Current $\overline{E}_0$, I_{0x}, I_{1x} S				20 40	V_{CC} = MAX, V_{IN} = 2.7V	μA
	Input HIGH Current at Max Input Voltage $\overline{E}_0$, I_{0x}, I_{1x} S				0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0V	mA
I_{IL}	Input LOW Current $\overline{E}_0$, I_{0x}, I_{1x} S				−0.4 −0.8	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CC}	Power Supply Current Outputs HIGH				10	V_{CC} = MAX, V_{IN} = 4.5V, $V_{\overline{E}}$ = 0V	mA
	Power Supply Current Outputs LOW				16	V_{CC} = MAX, V_{IN} = 0V, $V_{\overline{E}}$ = 0V	mA
	Power Supply Current Outputs Off				17	V_{CC} = MAX, V_{IN} = 0V, $V_{\overline{E}}$ = 4.5V	mA

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (T54LS/T74LS257A)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		I_{OH} = −1.0mA, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.4	3.1		I_{OH} = −2.6mA, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 24mA, V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.7V	μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_{OUT} = 0.4V	μA
I_{IH}	Input HIGH Current	Other Inputs S Inputs			20 40	V_{CC} = MAX, V_{IN} = 2.7V	μA
		Other Inputs S Input			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0V	mA
I_{IL}	Input LOW Current	Other Inputs S Input			−0.4 −0.8	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−30		−130	V_{CC} = MAX	mA
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW Total, Output 3-State				 10 16 19	V_{CC} = MAX	mA

Notes:

1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS: $T_A = 25°C$ (T54LS/T74LS257)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output			18 14	Fig. 1	$C_L = 15pF$	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output			21 21	Fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level			28	Figs. 4,5	$C_L = 15pF$ $R_L = 2\ k\Omega$	ns
t_{PZL}	Output Enable Time to LOW Level			24	Figs. 3,5		ns
t_{PLZ}	Output Disable Time from LOW Level			22	Figs. 3,5	$C_L = 5pF$ $R_L = 2\ k\Omega$	ns
t_{PHZ}	Output Disable Time from HIGH Level			14	Figs. 4,5		ns

AC CHARACTERISTICS: $T_A = 25°C$ (T54LS/T74LS257A)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		9 11	18 18	Fig. 1	$V_{CC} = 5.0V$ $C_L = 45pF$ $R_L = 667\ \Omega$	ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		16 19	21 25	Fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level		17	30	Figs. 4,5		ns
t_{PZL}	Output Enable Time to LOW Level		17	30	Figs. 3,5		ns
t_{PLZ}	Output Disable Time from LOW Level		15	25	Figs. 3,5	$V_{CC} = 5.0V$ $C_L = 5pF$	ns
t_{PHZ}	Output Disable Time from HIGH Level		17	30	Figs. 4,5		ns

WAVEFORMS

Fig. 1

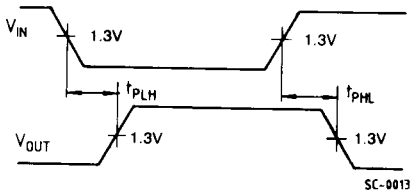


Fig. 2

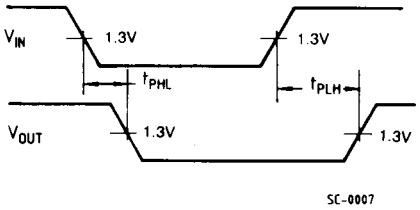


Fig. 3

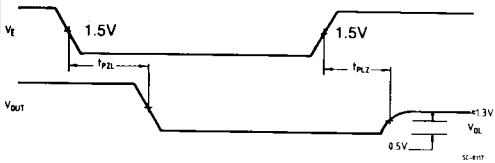


Fig. 4

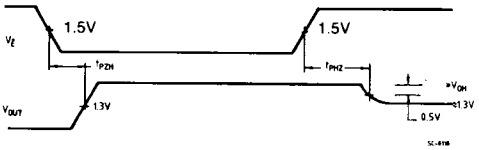
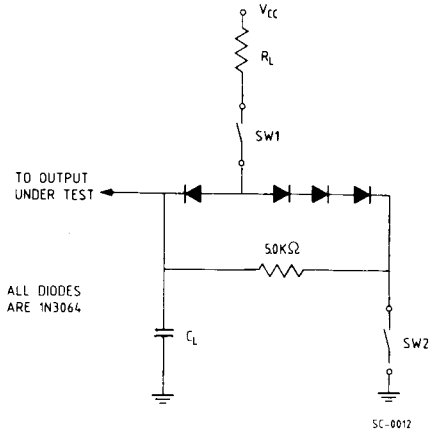


Fig. 5

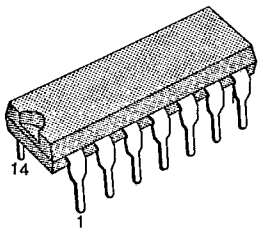


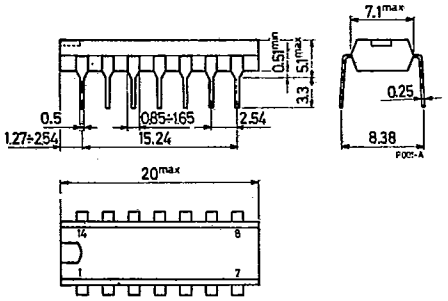
SWITCHING POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

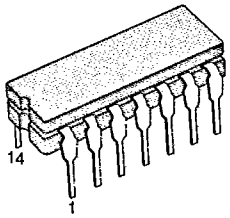
Packages

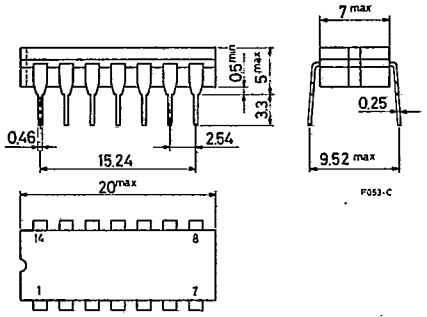
14-LEAD PLASTIC DIP





14-LEAD CERAMIC DIP





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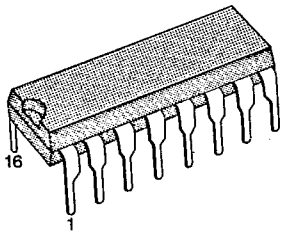
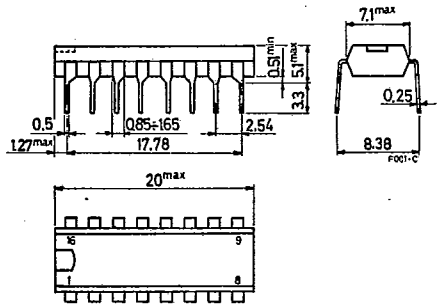
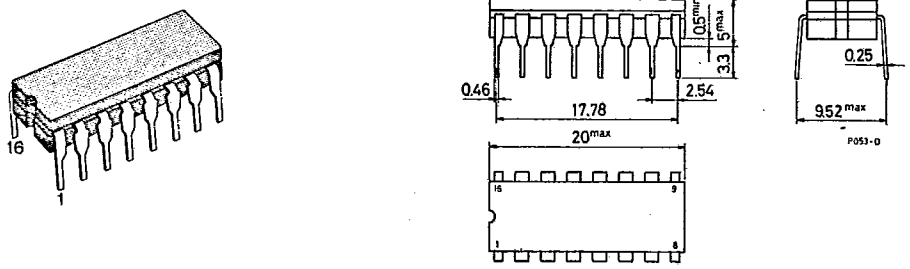




Packages

16-LEAD CERAMIC DIP



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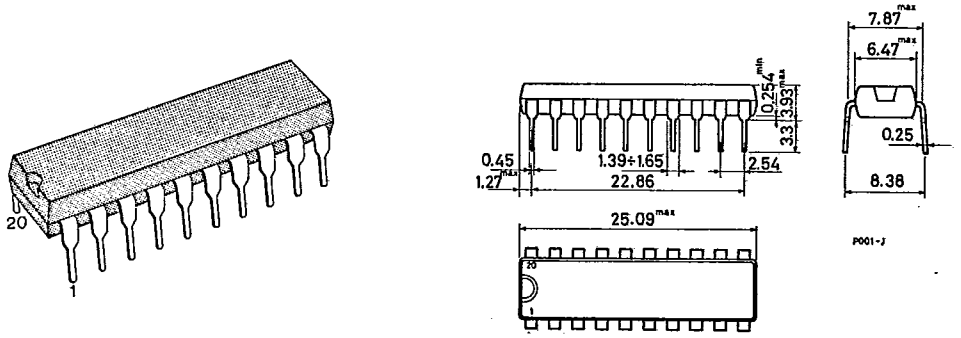

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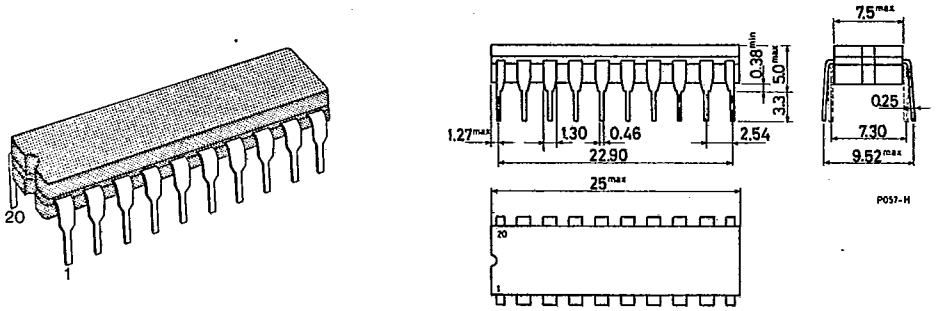
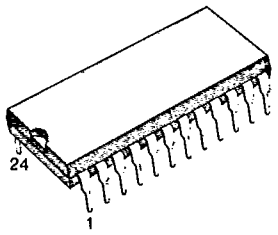
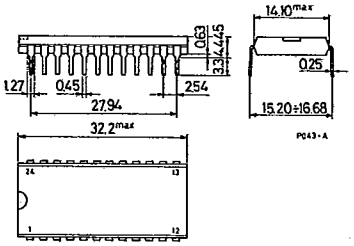


Packages

24-LEAD PLASTIC DIP





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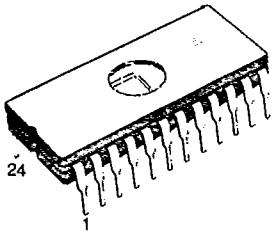
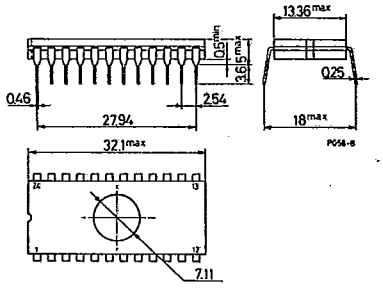
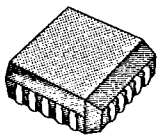
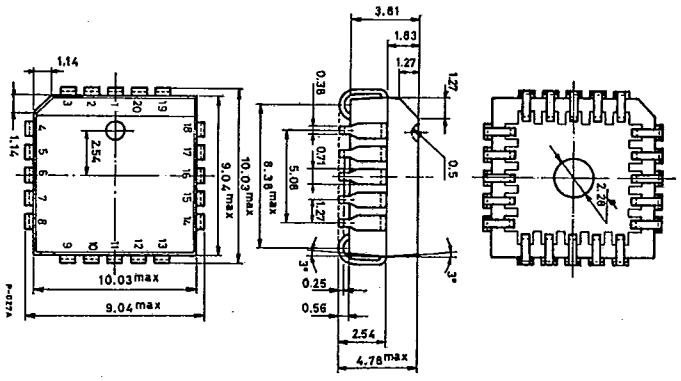




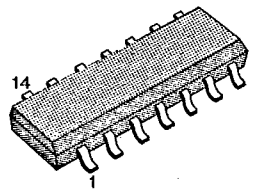
CHIP CARRIER 20 LEAD PLASTIC

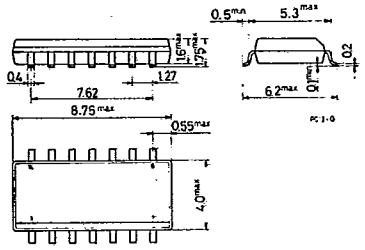




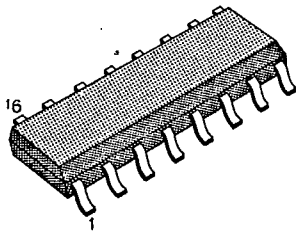
Packages

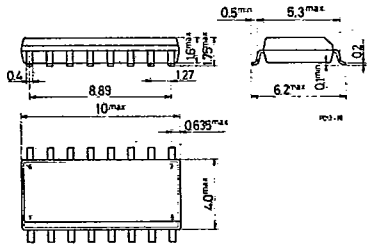
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.