



DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION

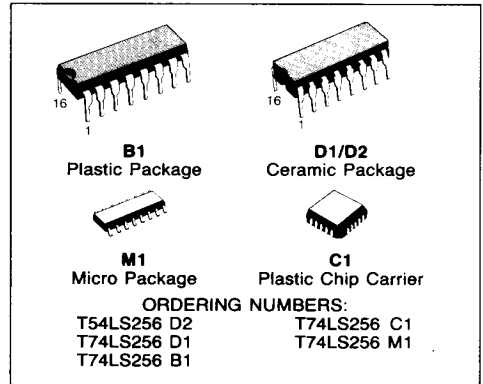
The T54LS256/T74LS256 is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address inputs (A_0, A_1), an active LOW Enable input (\bar{E}) and an active LOW Clear input (\bar{C}). Each latch has a Data input (D) and four outputs (Q_0-Q_3).

When the Enable (\bar{E}) is HIGH and the Clear input (\bar{C}) is LOW, all outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the \bar{C} and \bar{E} are both LOW. When \bar{C} is HIGH and \bar{E} is LOW, the selected outputs (Q_0-Q_3), determined by the Address inputs, follows D. When the \bar{E} goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\bar{E} = \text{LOW}$, $\bar{C} = \text{HIGH}$), changing more than one bit of the Address (A_0, A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\bar{E} = \bar{C} = \text{HIGH}$).

- SERIAL-TO-PARALLEL CAPABILITY
- OUTPUT FROM EACH STORAGE BIT AVAILABLE
- RANDOM (ADDRESSABLE) DATA ENTRY
- EASILY EXPANDABLE
- ACTIVE LOW COMMON CLEAR
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

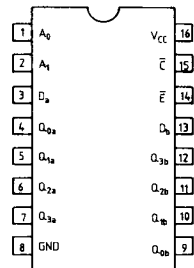
PIN NAMES

A_0, A_1	Address Inputs
D_a, D_b	Data Inputs
\bar{E}	Enable (Active LOW) Input
\bar{C}	Clear (Active LOW) Input
$Q_{0a}-Q_{3a}, Q_{0b}-Q_{3b}$	Parallel Latch Outputs



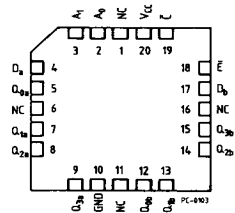
PIN CONNECTION (top view)

DUAL IN LINE



PC-0141

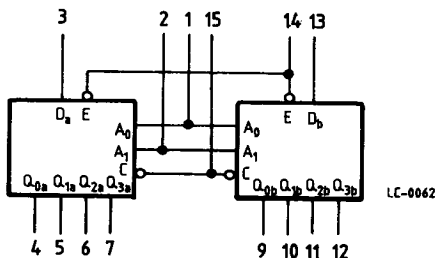
CHIP CARRIER



NC = No Internal Connection



LOGIC SYMBOL



MODE SELECTION

\bar{E}	\bar{C}	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Dual 4-Channel Demultiplexer
H	L	Clear

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	Input Voltage, Applied to Input	-0.5 to 15	V
V_O	Output Voltage, Applied to Output	-0.5 to 10	V
I_I	Input Current, Into Inputs	-30 to 5	mA
I_O	Output Current, Into Outputs	30	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

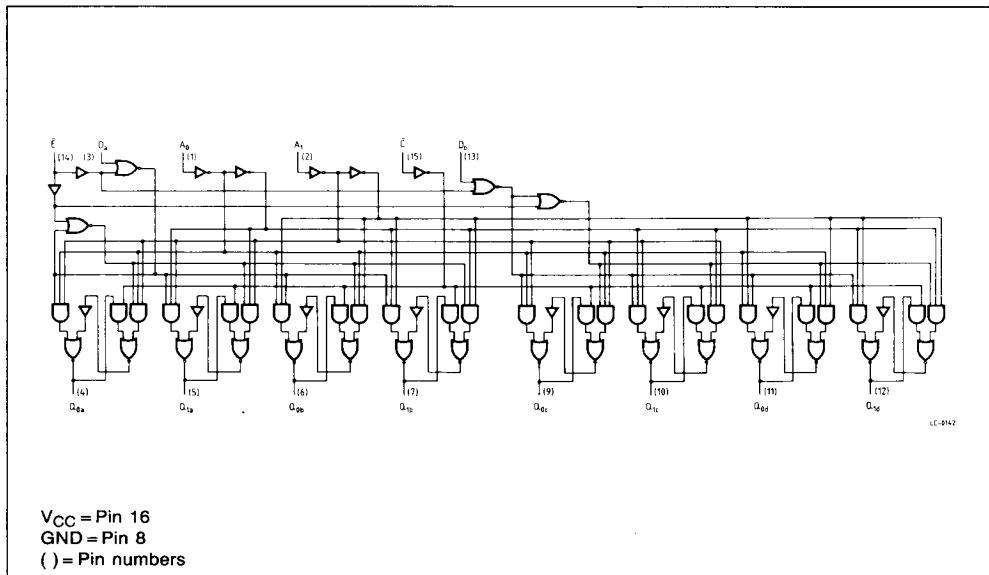
GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS256D2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS256XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.



LOGIC DIAGRAM



TRUTH TABLE

\bar{C}	\bar{E}	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	MODE
L	H	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplexer
L	L	H	L	L	H	L	L	L	
L	L	L	H	L	L	L	L	L	
L	L	H	H	L	L	H	L	L	
L	L	L	L	H	L	L	H	L	
L	L	H	H	H	L	L	L	L	
L	L	L	H	H	L	L	L	H	
L	L	H	H	H	L	L	L	H	
H	H	X	X	X	Q_{n-1}	Q_{n-1}	Q_{n-1}	Q_{n-1}	Memory
H	L	L	L	L	L	Q_{n-1}	Q_{n-1}	Q_{n-1}	Addressable Latch
H	L	H	L	L	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	
H	L	L	H	L	Q_{n-1}	L	Q_{n-1}	Q_{n-1}	
H	L	H	H	L	Q_{n-1}	H	Q_{n-1}	Q_{n-1}	
H	L	L	L	H	Q_{n-1}	Q_{n-1}	L	Q_{n-1}	
H	L	H	L	H	Q_{n-1}	Q_{n-1}	H	Q_{n-1}	
H	L	L	H	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	L	
H	L	H	H	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	H	

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units
			Min.	Typ.	Max.		
V _{IH}	Input HIGH Voltage		2.0			Guaranteed input Logical HIGH Voltage for all Inputs	V
V _{IL}	Input LOW Voltage	54			0.7	Guaranteed input Logical LOW Voltage for all Inputs	V
		74			0.8		
V _{CD}	Input Clamp Diode Voltage				-1.5	V _{CC} = MIN, I _{IN} = -18mA	V
V _{OH}	Output HIGH Voltage	54	2.4	3.4		V _{CC} = MIN, I _{OH} = -400μA, V _{IN} = V _{IH} or V _{IL} per Truth Table	V
		74	2.4	3.1			
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table	V
		74		0.35	0.5		
I _{IH}	Input HIGH Current A ₀ , A ₁ , C̄, D _a , D _b E				20 40	V _{CC} = MAX, V _{IN} = 2.7V	μA
	Input HIGH Current A ₀ , A ₁ , C̄, D _a , D _b E				0.1 0.2	V _{CC} = MAX, V _{IN} = 7.0V	mA
I _{IL}	Input LOW Current A ₀ , A ₁ , C̄, D _a , D _b E				-0.4 -0.8	V _{CC} = MAX, V _{IN} = 0.4V	mA
I _{OS}	Output Short Circuit Current (Note 2)		-20		-100	V _{CC} = MAX, V _{OUT} = 0V	mA
I _{CC}	Power Supply Current			20	25	V _{CC} = MAX	mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter		Limits			Test Conditions	Units
			Min.	Typ.	Max.		
t _{PLH}	Turn-Off Delay, Enab. to Out.			20	27	Fig. 1	ns
t _{PHL}	Turn-On Delay, Enab. to Out.			16	24		
t _{PLH}	Turn-Off Delay, Data to Output			20	30	Fig. 2	V _{CC} = 5.0V C _L = 15pF
t _{PHL}	Turn-On Delay, Data to Output			13	20		
t _{PLH}	Turn-Off Delay, Addr. to Outp.			20	30	Fig. 3	
t _{PHL}	Turn-On Delay, Addr. to Outp.			14	24		
t _{PHL}	Turn-On Delay, Clear to Output			12	23	Fig. 5	

Notes:

- 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at V_{CC} = 5.0V, T_A = 25°C



AC SET-UP REQUIREMENTS: $T_A = 25^\circ\text{C}$

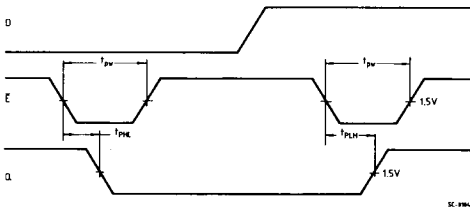
Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{sH}	Set-up Time HIGH, Data to Enable	20	13		$V_{CC} = 5.0V$	Fig. 4	ns
t_{hH}	Hold Time HIGH, Data to Enable	0	-7.0				
t_{sL}	Set-up Time LOW, Data to Enable	15	7.0				
t_{hL}	Hold Time LOW, Data to Enable	0	10				
$t_{sA-\bar{E}}$	Set-up Time, Address to Enable (Note 4)	0	-7.0		$V_{CC} = 5.0V$	Fig. 6	ns
$t_{W\bar{E}}$	Enable Pulse Width	17	12		$V_{CC} = 5.0V$	Fig. 1	ns

Notes:

- 4) The address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- 5) The shaded areas indicate when the inputs are permitted to change for predictable output performance.

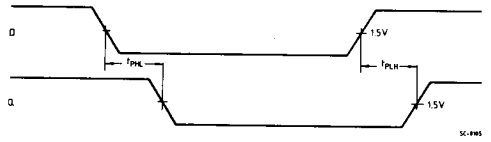
AC WAVEFORMS

Fig. 1 Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width

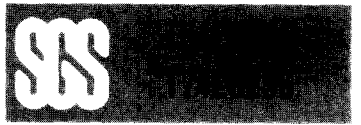


OTHER CONDITIONS: $\bar{C} = H, A = \text{STABLE}$

Fig. 2 Turn-On and Turn-Off Delays, Data to Output

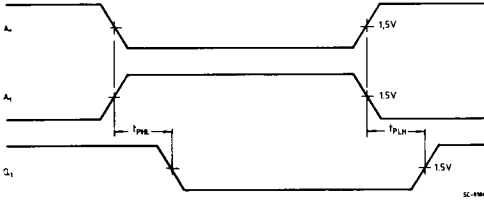


OTHER CONDITIONS: $\bar{E} = L, \bar{C} = H, A = \text{STABLE}$



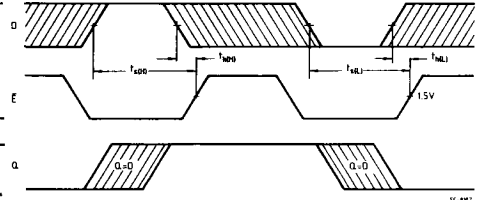
AC WAVEFORMS (Continued)

Fig. 3 Turn-On and Turn-Off Delays, Address to Output



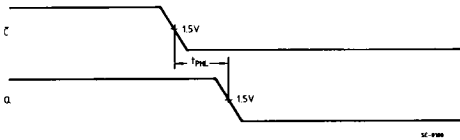
OTHER CONDITIONS: $\bar{E} = L, \bar{C} = L, D = H$

Fig. 4 Set-up and Hold Time, Data to Enable



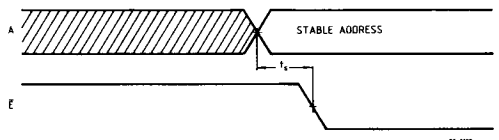
OTHER CONDITIONS: $\bar{C} = H, A = \text{STABLE}$

Fig. 5 Turn-On Delay, Clear to Output



OTHER CONDITIONS: $\bar{E} = H$

Fig. 6 Set-up Time, Address to Enable (see notes 4 and 5)



OTHER CONDITIONS: $\bar{C} = H$