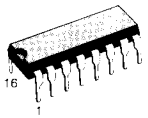
# T54LS194A
# T74LS194A

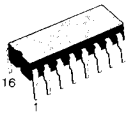
## 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

### DESCRIPTION

The T54LS194A/T74LS194A is a High Speed Bidirectional Universal Shift Register. As a high speed multifunctional sequential bulding block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194A is similar in operation to be LS195 Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all SGS TTL families.



**B1**
Plastic Package



**D1/D2**
Ceramic Package

**M1**
Micro Package

**C1**
Plastic Chip Carrier

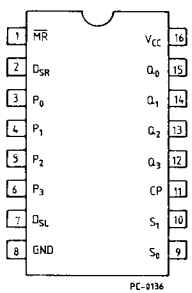
ORDERING NUMBERS:

T54LS194A D2
T74LS194A D1
T74LS194A B1
T74LS194A C1
T74LS194A M1

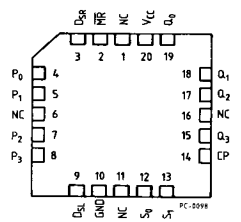
- TYPICAL SHIFT REGISTER FREQUENCY OF 40 MHz
- ASYCHRONOUS MASTER RESET
- HOLD (DO NOTHING) MODE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

### PIN CONNECTION
(top view)

DUAL IN LINE




CHIP CARRIER

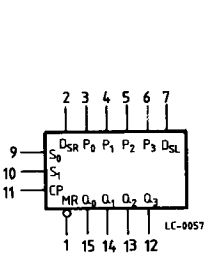


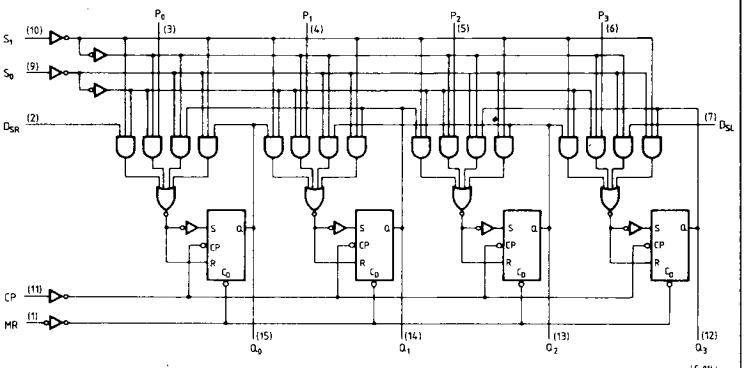

NC = No Internal Connection

### PIN NAMES

| | |
|---|---|
| $S_0$-$S_1$ | Mode Control to Input |
| $P_0$-$P_3$ | Parallel Data Inputs |
| $D_{SR}$ | Serial (Shift Right) Data Input |
| $D_{SL}$ | Serial (Shift Left) Data Input |
| CP | Clock (Active HIGH Going Edge) Input |
| $\overline{MR}$ | Master Reset (Active LOW) Input |
| $Q_0$-$Q_3$ | Parallel Outputs |

## LOGIC SYMBOL AND LOGIC DIAGRAM




$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin numbers

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to 7 | V |
| $V_I$ | Input Voltage, Applied to Input | −0.5 to 5.5 | V |
| $V_O$ | Output Voltage, Applied to Output | −0.5 to 5.5 | V |
| $I_I$ | Input Current, Into Inputs | −30 to 5 | mA |
| $I_O$ | Output Current, Into Outputs | 50 | mA |

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## GUARANTEED OPERATING RANGES

| Part Numbers | Supply Voltage | | | Temperature |
|---|---|---|---|---|
| | Min | Typ | Max | |
| T54LS194AD2 | 4.5 V | 5.0 V | 5.5 V | −55°C to +125°C |
| T74LS194AXX | 4.75 V | 5.0 V | 5.25 V | 0°C to +70°C |

XX = package type.

## MODE SELECT - TRUTH TABLE

| OPERATING MODE | INPUTS | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | $S_1$ | $S_0$ | $D_{SR}$ | $D_{SL}$ | $P_n$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| Reset | L | X | X | X | X | X | L | L | L | L |
| Hold | H | l | l | X | X | X | $q_0$ | $q_1$ | $q_2$ | $q_3$ |
| Shift Left | H | h | l | X | l | X | $q_1$ | $q_2$ | $q_3$ | L |
| | H | h | l | X | h | X | $q_1$ | $q_2$ | $q_3$ | H |
| Shift Right | H | l | h | l | X | X | L | $q_0$ | $q_1$ | $q_2$ |
| | H | l | h | h | X | X | H | $q_0$ | $q_1$ | $q_2$ |
| Parallel Load | H | h | h | X | X | $P_n$ | $P_0$ | $P_1$ | $P_2$ | $P_3$ |

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition
$P_n$ ($q_n$) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

### FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the 194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the LS195A Universal Shift Register when used in seral or parallel data register transfers. Some of the common features of the two devices are described below:

1) All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.
2) The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implmenting very high speed CPUs, or the memory buffer registers.
3) The four parallel dat inputs ($P_0$, $P_1$, $P_2$, $P_3$) are D-type inputs. When both $S_0$ and $S_1$ are HIGH, the data appearing on $P_0$, $P_1$, $P_2$ and $P_3$ inputs is transferred to the $Q_0$, $Q_1$, $Q_2$ and $Q_3$ outputs respectively following the next LOW to HIGH transition of the clock.
4) The asychronous Master Reset ($\overline{MR}$), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

1) Two mode control inputs ($S_0$, $S_1$) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both $S_0$ and $S_1$ are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.
2) D-type seral data inputs ($D_{SR}$, $D_{SL}$) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Symbol | Parameter | | Limits Min. | Limits Typ. | Limits Max. | Test Conditions (Note 1) | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | Guaranteed input HIGH Voltage for all Inputs | V |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | Guaranteed input LOW Voltage for all Inputs | V |
| | | 74 | | | 0.8 | | |
| $V_{CD}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | V |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | 3.4 | | $V_{CC}$ = MIN, $I_{OH}$ = −400μA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | V |
| | | 74 | 2.7 | 3.4 | | | |
| $V_{OL}$ | Output LOW Voltage | 54,74 | | 0.25 | 0.4 | $I_{OL}$ = 4.0mA; $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | V |
| | | 74 | | 0.35 | 0.5 | $I_{OL}$ = 8.0mA | |
| $I_{IH}$ | Input HIGH Current | | | | 20<br>0.1 | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V<br>$V_{CC}$ = MAX, $V_{IN}$ = 7.0V | μA<br>mA |
| $I_{IL}$ | Input LOW Current | | | | −0.4 | $V_{CC}$ = MAX, $V_{IN}$ = 0.4V | mA |
| $I_{OS}$ | Output Short Circuit Current (Note 2) | | −20 | | −100 | $V_{CC}$ = MAX, $V_{OUT}$ = 0V | mA |
| $I_{CC}$ | Power Supply Current | | | 15 | 23 | $V_{CC}$ = MAX | mA |

## AC CHARACTERISTICS: $T_A$ = 25°C

| Symbol | Parameter | Limits Min. | Limits Typ. | Limits Max. | Test Conditions | | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Shift Frequency | 25 | 36 | | Fig. 1 | $V_{CC}$ = 5.0V<br>$C_L$ = 15pF | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, Clock to Output | | 14<br>17 | 22<br>26 | Fig. 1 | | ns |
| $t_{PLH}$ | Propagation Delay, $\overline{MR}$ to Output | | 19 | 30 | Fig. 2 | | ns |

**Notes:**
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at $V_{CC}$ = 5.0V, $T_A$ = 25°C

## AC SET-UP REQUIREMENTS: $T_A = 25°C$

| Symbol | Parameter | Limits | | | Test Conditions | | Units |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| $t_W(CP)$ | Clock Pulse Width | 20 | | | Fig. 1 | $V_{CC} = 5.0V$ | ns |
| $t_s(Data)$ | Set-up Time Data to Clock | 20 | | | Fig. 3 | | ns |
| $t_h(Data)$ | Hold Time Data to Clock | 0 | | | | | ns |
| $t_s(S)$ | Set-up Time Mode Control to Clock | 30 | | | Fig. 4 | | ns |
| $t_s(S)$ | Hold Time Mode, Control to Clock | 0 | | | | | ns |
| $t_W(\overline{MR})$ | Master Reset Pulse Width | 20 | | | Fig. 2 | | ns |
| $t_{rec}(\overline{MR})$ | Recovery Time Master Reset to Clock | 25 | | | | | ns |

### DEFINITION OF TERMS:

SET-UP TIME ($t_s$) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

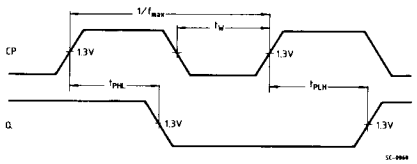
HOLD TIME ($t_h$) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME ($t_{rec}$) - is defined as the minimim time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognized and transfer HIGH Data to the Q outputs.

## AC WAVEFORMS

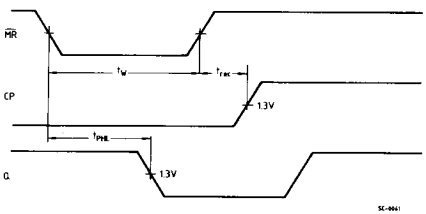
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 1 Clock to Output Delays
Clock Pulse Width and $f_{max}$




OTHER CONDITIONS: $S_1 = L$, $\overline{MR} = H$, $S_0 = H$

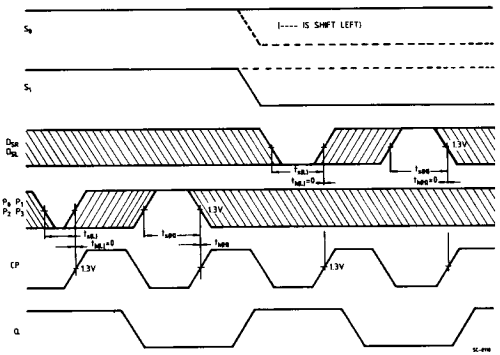
Fig. 2 Master Reset Pulse Width,
Master Reset to Output Delay and
Master Reset to Clock Recovery Time




OTHER CONDITIONS: $S_0$, $S_1 = H$
$P_0 = P_1 = P_2 = P_3 = H$

## AC WAVEFORMS (continued)

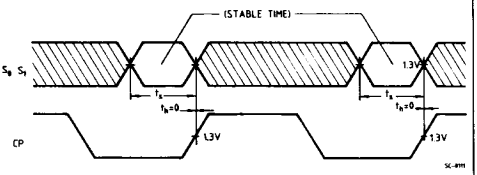
Fig. 3 Set-up ($t_s$) and Hold ($t_h$) Time for Serial Data ($D_{SR}$, $D_{SL}$) and Parallel Data ($P_0$, $P_1$, $P_2$, $P_3$)




OTHER CONDITIONS: $\overline{MR}$ = H

* $D_{SR}$ set-up time affects $Q_0$ only $D_{SL}$ set-up time affects $Q_3$ only

Fig. 4Set-up ($t_s$) and Hold ($t_h$) Time for S Input




OTHER CONDITIONS: $\overline{MR}$ = H