T54LS192/193
T74LS192/193

LS192 - PRESETTABLE BCD/DECADE UP/DOWN COUNTER
LS193 - PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

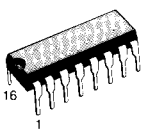
DESCRIPTION

The T54LS192/T74LS192 is a UP/DOWN BCD Decade (8421) Counter and the T54LS193/T74LS193 is an UP/DOWN Modulo-16 Binary Counter. Separate Count Down Clocks are used an in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW to HIGH transitions on the clock inputs.
Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clock for subsequent stages without extra logic, thus simplifying multistage counter designs.
individual preset inputs allow the circuits to be used as programmable counters. Both the parallel Load ($\overline{PL}$) and the Master Reset inputs asynchronously override the clock.

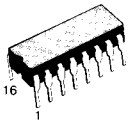
- LOW POWER 95 mW TYPICAL DISSIPATION
- SYNCHRONOUS COUNTING
- CASCADING CIRCUITRY INTERNALLY PROVIDED
- ASYNCHRONOUS MASTER RESET AND PARALLEL LOAD
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- HIGH SPEED 40 MHz TYPICAL COUNT FREQUENCY
- INDIVIDUAL PRESET INPUTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

CP_U	Count Up Clock Pulse Input
CP_D	Count Down Clock Pulse Input
MR	Asynchronous Master reset (Clear) Input
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input
P_n	Parallel Data Inputs
Q_n	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output
$\overline{TC}_U$	Terminal Count Up (Carry) Output



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

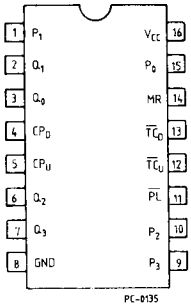
C1
Plastic Chip Carrier

ORDERING NUMBERS:

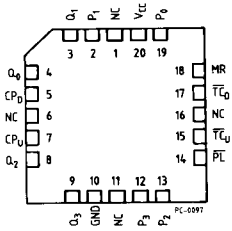
T54LSXXX D2
T74LSXXX D1
T74LSXXX B1
T74LSXXX C1
T74LSXXX M1

PIN CONNECTION
(top view)

DUAL IN LINE

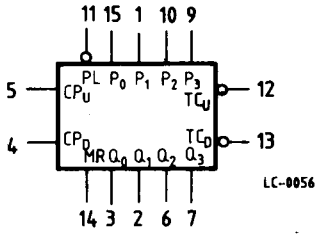


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND STATE DIAGRAMS



LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \bullet Q_3 \bullet \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$

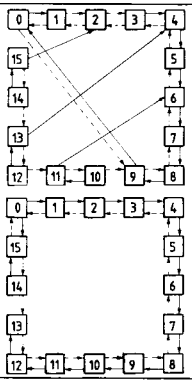
LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$

COUNT UP ⟶

COUNT DOWN ----▶



MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asynchronous)
L	L	X	X	Preset (Asynchronous)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⌐ = LOW to HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

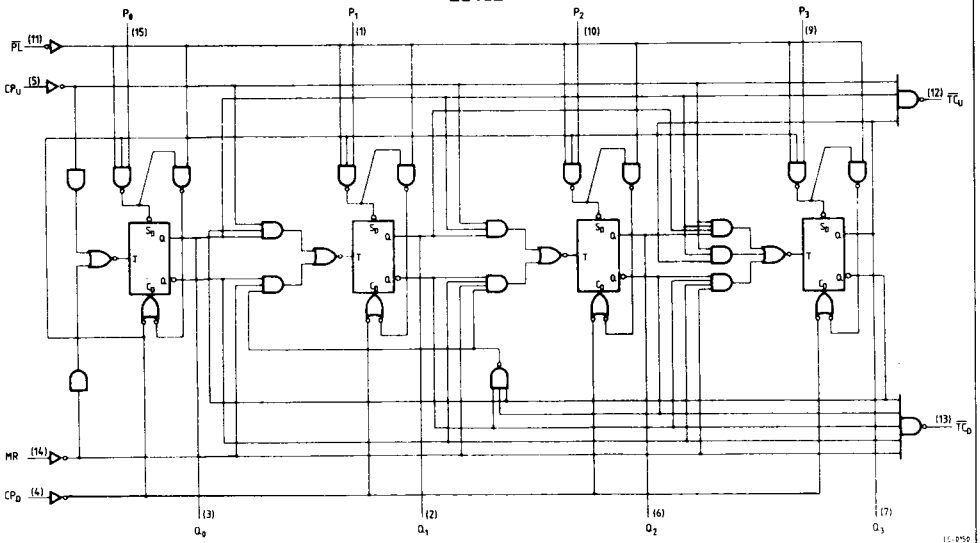
GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS192/193D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS192/193XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

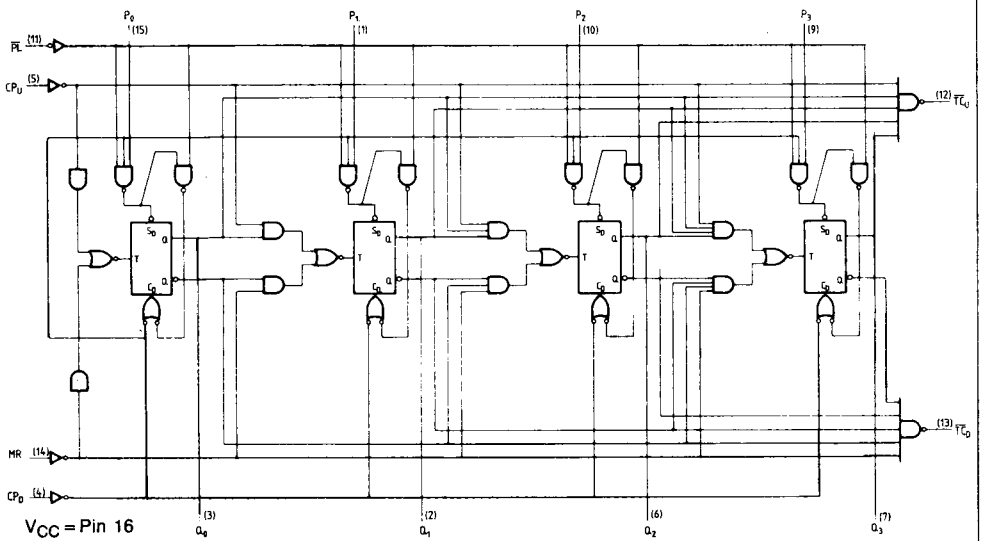
XX = package type.

LOGIC DIAGRAMS

DECADE COUNTER
LS192



BINARY COUNTER
LS193



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

FUNCTIONAL DESCRIPTION

The LS192 and 193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversable) Counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up an count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up inut will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW. The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 5 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays.
Similary, the $\overline{TC}_D$ output will go to LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has and asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the present gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)		Units
			Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table		V
		74	2.7	3.4				
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V		μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current			19	34	V_{CC} = MAX		mA

AC CHARACTERISTICS: T_A = 25°C (LS192/193)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Max Input Count Frequency	25	32		Fig. 1	V_{CC} = 5.0V C_L = 15pF	ns
t_{PLH} t_{PHL}	CP_U Input to $\overline{TC}_U$ Output		17 18	26 24	Fig. 2		ns
t_{PLH} t_{PHL}	CP_D Input to $\overline{TC}_D$ Output		16 15	24 24			ns
t_{PLH} t_{PHL}	CP_U or CP_D to Q_n Outputs		17 30	38 47			ns
t_{PLH} t_{PHL}	$\overline{PL}$ Inputs to Any Outputs		24 25	40 40	Fig. 4		ns
t_{PHL}	MR Input to Any Output		23	35	Fig. 17		ns

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (LS192/LS193)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_W	CP_U Pulse Width	20			Fig. 1	$V_{CC} = 5.0V$	ns
t_W	PL_D Pulse Width	20					ns
t_W	$\overline{PL}$ Pulse Width	20			Fig. 4		ns
t_W	MR Pulse Width	20					ns
t_sL	Set-up Time LOW, Data to $\overline{PL}$	20			Fig. 6		ns
t_hL	Hold Time LOW, Data to $\overline{PL}$	50					ns
t_sH	Set-up Time HIGH, Data to $\overline{PL}$	20					ns
t_hH	Hold Time HIGH Data to $\overline{PL}$	5					ns
t_{rec}	Recovery Time	40			Fig. 5		ns

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the $\overline{PL}$ transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the $\overline{PL}$ transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the $\overline{PL}$ transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) - is defined as the minimim time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

Fig. 1

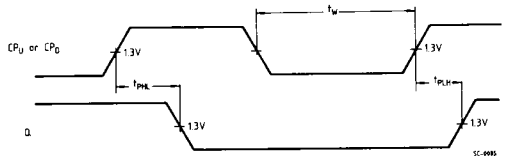


Fig. 2

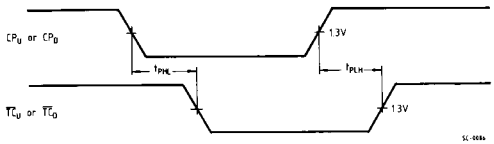
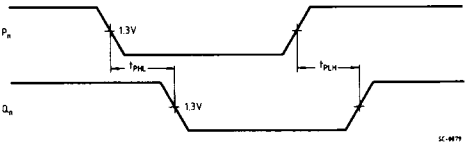


Fig. 3



NOTE: $\overline{PL}$ = LOW

Fig. 4

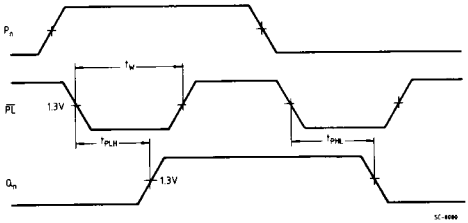


Fig. 5

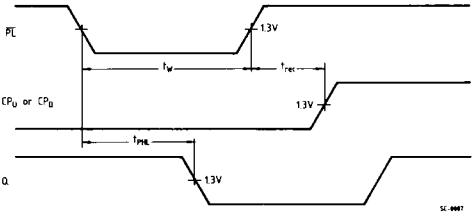


Fig. 6

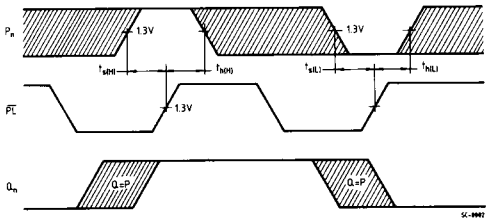
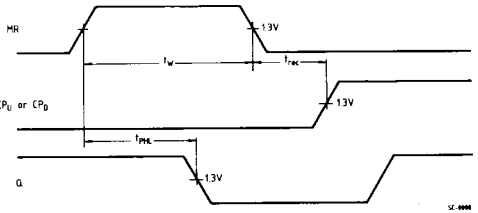


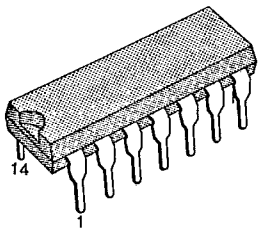
Fig. 7

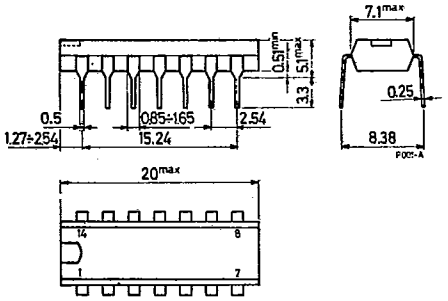


* The Shaded areas indicate when the input is permitted to change for predictable output performance.

Packages

14-LEAD PLASTIC DIP





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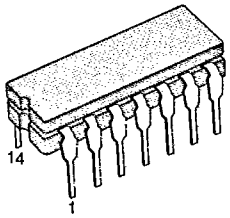

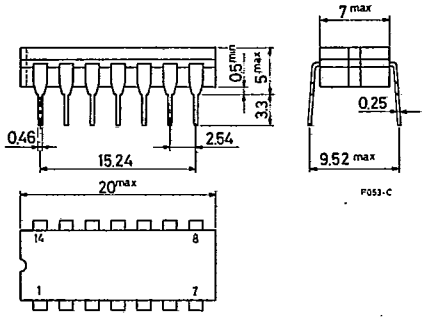

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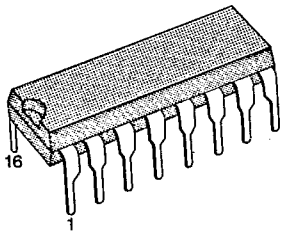

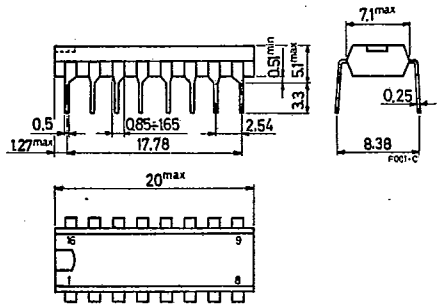

Packages

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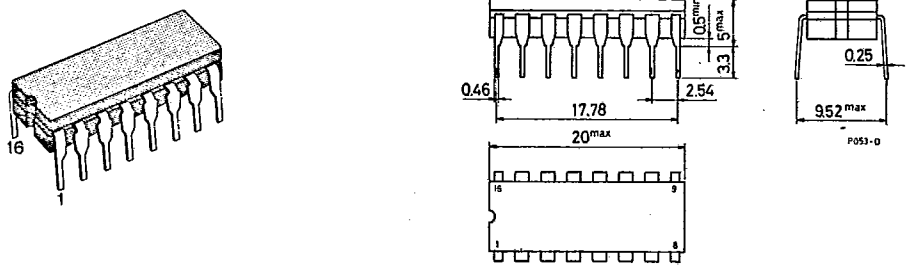

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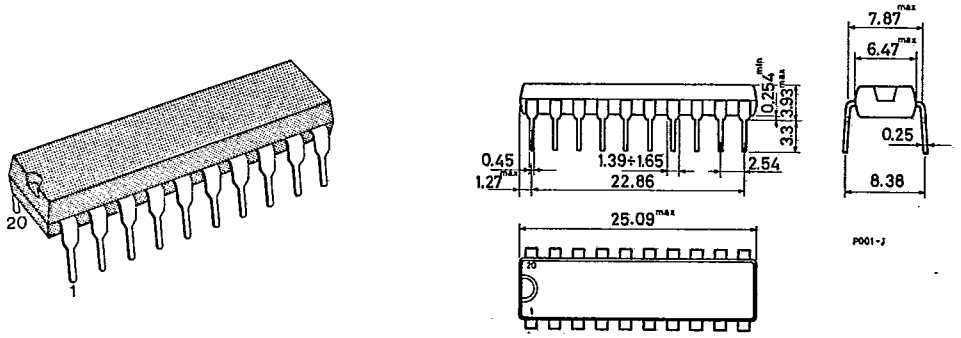

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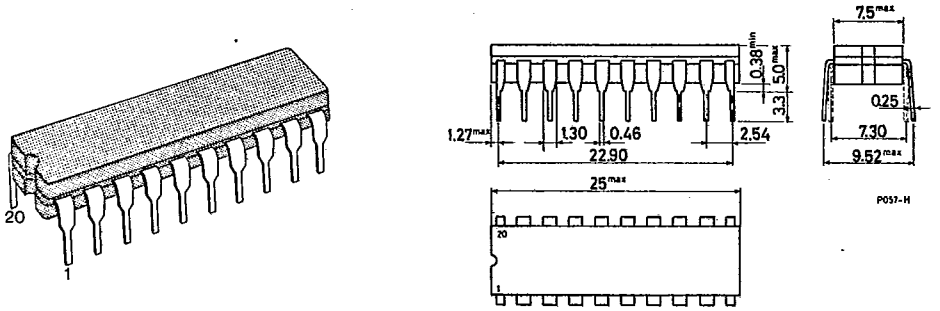

Packages

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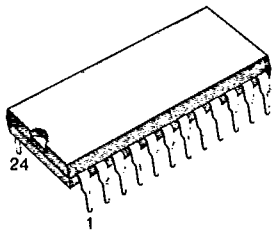

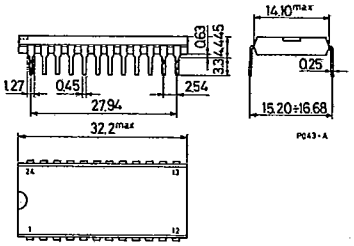

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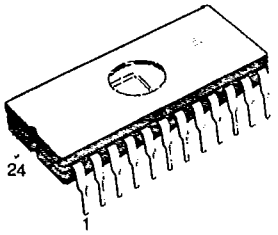
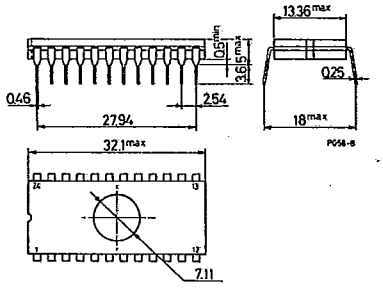
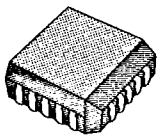
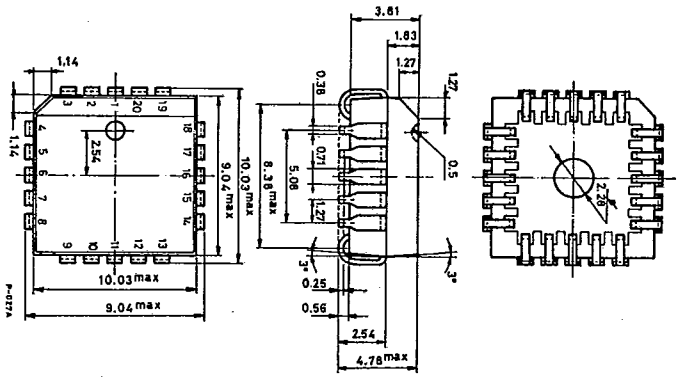




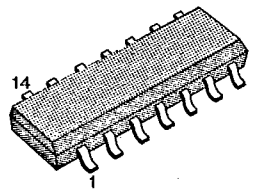
CHIP CARRIER 20 LEAD PLASTIC

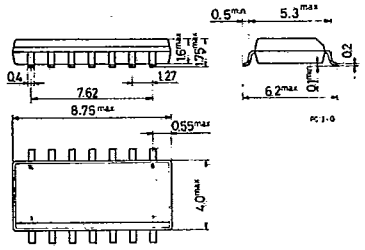




Packages

14-LEAD PLASTIC DIP MICROPACKAGE





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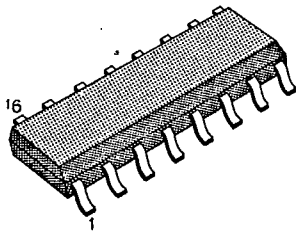

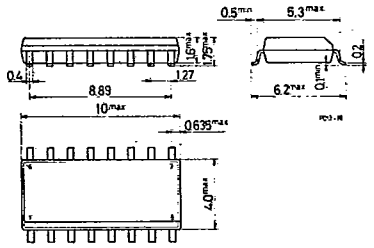

NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.