

T54LS190/191
T74LS190/191



LS190 - PRESETTABLE BCD/DECADE UP/DOWN COUNTERS
LS191 - PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

DESCRIPTION

The T54LS190/T74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the T54LS191/T74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load (PL) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters.

A Count Enable (CE) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control (U/D) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock (RC) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multi-stage counter applications.

- LOW POWER 90 mW TYPICAL DISSIPATION
- SYNCHRONOUS COUNTING
- INDIVIDUAL PRESET INPUTS
- CASCADABLE
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- HIGH SPEED 35 MHz TYPICAL COUNT FREQUENCY
- ASYNCHRONOUS PARALLEL LOAD
- COUNT ENABLE AND UP/DOWN CONTROL INPUT
- FULLY TTL AND CMOS COMPATIBLE

B1
Plastic Package

D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
T54LSXXX D2 T74LSXXX C1
T74LSXXX D1 T74LSXXX M1
T74LSXXX B1

PIN CONNECTION
(top view)

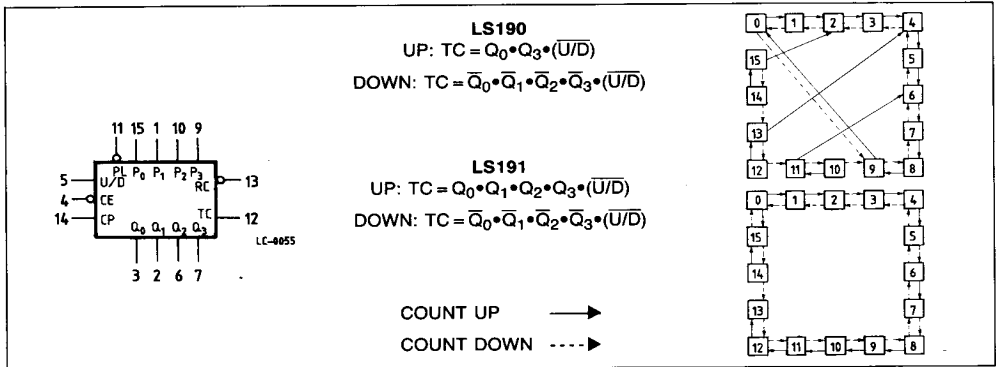
DUAL IN LINE

CHIP CARRIER

NC = No Internal Connection



LOGIC SYMBOL AND STATE DIAGRAMS



MODE SELECT TABLE

INPUTS				MODE
\overline{PL}	\overline{CE}	$\overline{U/D}$	CP	
H	L	L	\downarrow	Count Up
H	L	H	\downarrow	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			RC OUTPUT
\overline{CE}	TC*	CP	
L	H	\downarrow	\downarrow
H	X	X	H
X	L	X	H

* TC is generated internally

L = LOW Voltage Level, H = HIGH Voltage Level, X = Don't Care, \downarrow = LOW to HIGH clock transition, \downarrow = LOW Pulse

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	Input Voltage, Applied to Input	-0.5 to 15	V
V_O	Output Voltage, Applied to Output	-0.5 to 10	V
I_I	Input Current, Into Inputs	-30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS190/191D2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS190/191XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

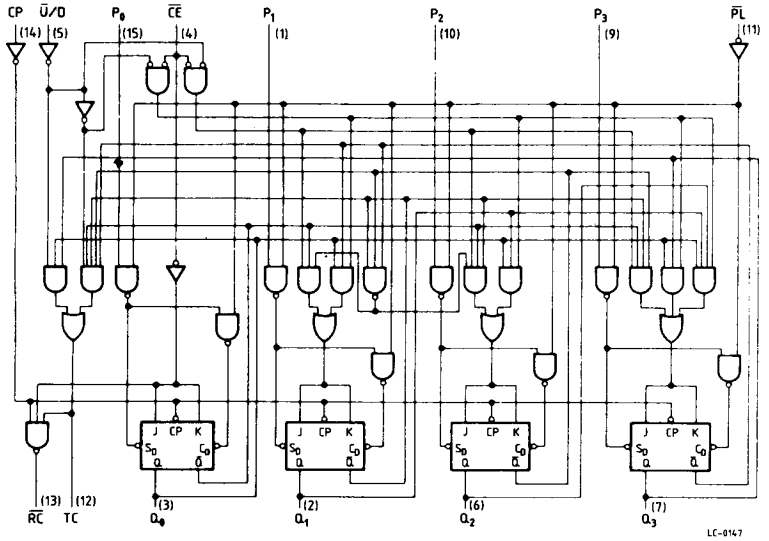
XX = package type.



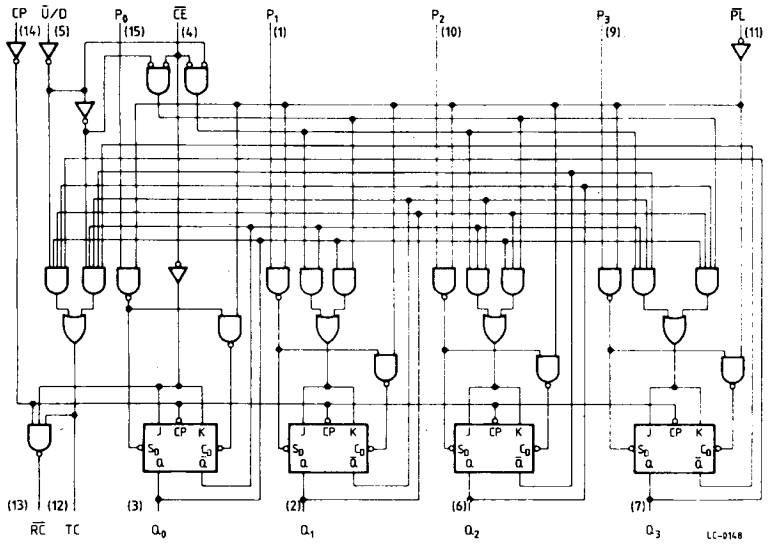
T54LS100/191
T74LS190/191

LOGIC DIAGRAMS

DECADE COUNTER
LS190



BINARY COUNTER
LS191



V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

FUNCTIONAL DESCRIPTION

The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four masters slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (PL) input is LOW, information present on the Parallel Data inputs (P₀-P₃) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the \overline{CE} input inhibits counting. When \overline{CE} is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U/D}$ input signal, as indicated in the Mode Select Table. When counting is to be enabled, the \overline{CE} signal can be made LOW when the clock is in either state.

However, when counting is to be inhibited, the LOW-to-HIGH \overline{CE} transition must occur only while the clock is HIGH. Similarly, the $\overline{U/D}$ signal should only be changed when either \overline{CE} or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U/D}$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (\overline{RC}) output. The \overline{RC} output is normally HIGH. When \overline{CE} is LOW and TC is HIGH, the \overline{RC} output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each \overline{RC} output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on \overline{CE} inhibits the \overline{RC} output pulse, as indicated in the \overline{RC} Truth table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages.

This represents the cumulative delay of the clock as it ripples through the preceding stages. A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All Clock inputs are driven in parallel and the \overline{RC} outputs propagate the carry/borrow signals ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the \overline{RC} output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The \overline{CE} input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own \overline{CE} .

Fig. a) n-stage counter using ripple clock

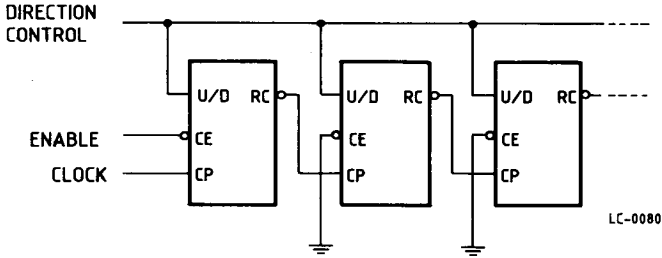


Fig. b) Synchronous n-stage counter using ripple carry/borrow

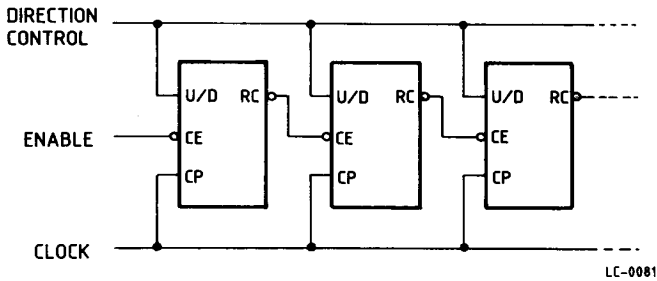
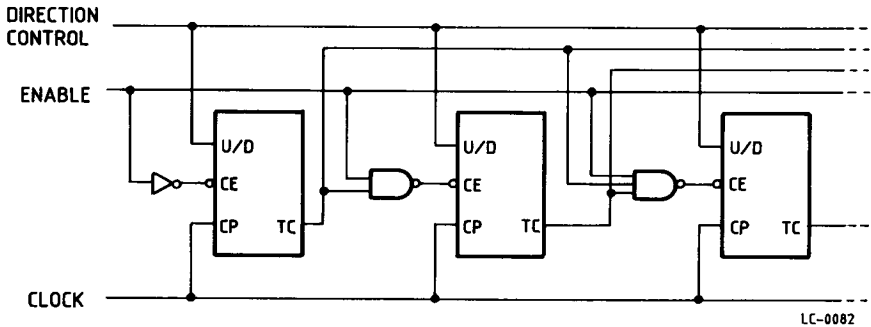


Fig. c) Synchronous n-stage counter with parallel gated carry/borrow



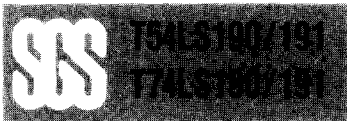


DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units
			Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$	V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		$V_{CC} = \text{MIN}, I_{OH} = -400\mu\text{A}, V_{IN} = V_{IH}$ or V_{IL} per Truth Table	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	$I_{OL} = 4.0\text{mA}$ $V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	V
		74		0.35	0.5		
I_{IH}	Input HIGH Current $P_0, \overline{PL}, CP, \overline{U/D}$ \overline{CE}				20 60	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$	μA
	$P_0, \overline{PL}, CP, \overline{U/D}$ \overline{CE}				0.1 0.3		
I_{IL}	Input LOW Current $P_0, \overline{PL}, CP, \overline{U/D}$ \overline{CE}				-0.4 -1.08	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$	mA
I_{OS}	Output Short Circuit Current (Note 2)		-20		-100	$V_{CC} = \text{MAX}, V_{OUT} = 0\text{V}$	mA
I_{CC}	Power Supply Current			20	35	$V_{CC} = \text{MAX}, \text{All Inputs } 0\text{V}$	mA

Notes:

- 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- 2) Not more than one output should be shorted at a time.
- 3) The Set-up Time " $t_s(H)$ " and Hold Time " $t_h(L)$ " between the Count Enable (\overline{CE}) and the clock (CP) indicate that the LOW-to-HIGH transition of the \overline{CE} must occur only while the Clock is HIGH for conventional operation.
- 4) Typical values are at $V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}$



AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f_{MAX}	Max Input Count frequency	20	25		Fig. 1	ns
t_{PLH} t_{PHL}	Propagation delay, CP Input to Q Output		16 24	24 36	Fig. 1	ns
t_{PLH} t_{PHL}	CP Input to \overline{RC} Output		13 16	20 24	Fig. 2	ns
t_{PLH} t_{PHL}	CP Input to TC Output		28 37	42 52	Fig. 1	ns
t_{PLH}^* t_{PHL}^*	$\overline{U/D}$ Input to \overline{RC} Output		30 30	45 45	Fig. 7	ns
t_{PLH} t_{PHL}^*	$\overline{U/D}$ Input to TC Output		21 22	33 33	Fig. 7	ns
t_{PLH} t_{PHL}	P_0 - P_3 Inputs to Q_0 - Q_3 Out.		20 27	32 40	Fig. 3	ns
t_{PLH} t_{PHL}	\overline{PL} Input to Any Output		22 33	33 50	Fig. 4	ns
t_{PLH}^* t_{PHL}	\overline{CE} Input to \overline{RC} Output		21 22	33 33	Fig. 2	ns

$V_{CC} = 5.0V$
 $C_L = 15pF$

* It is possible to get these timing relationship, but they should not occur during normal operation since the CP would be HIGH.

AC-SET UP REQUIREMENTS: $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_W	CP Pulse Width	25			Fig. 1	ns
t_W	PL Pulse Width	35			Fig. 4	ns
t_{sL}	Set-Up Time, LOW Data to PL	30			Fig. 6	ns
t_{hL}	Hold Time LOW, Data to PL	5				ns
t_{sH}	Set-up Time HIGH, Data to PL	30				ns
t_{hH}	Hold Time HIGH, Data to PL	5				ns
t_{rec}	Recovery Time, PL to CP	40			Fig. 5	ns
t_{sL}	Set-up Time LOW, CE to Clock	30			Fig. 8	ns
t_{hL}	Hold Time LOW, CE to Clock	5				ns

$V_{CC} = 5.0V$

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to be recognized and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

Fig. 1

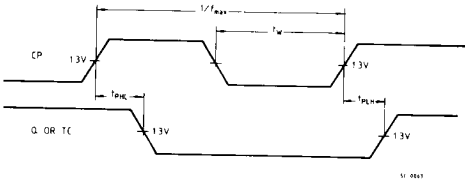


Fig. 2

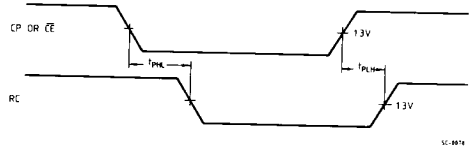
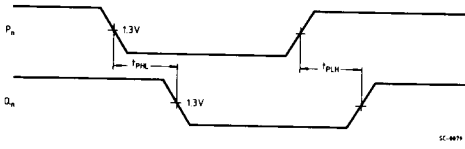


Fig. 3



NOTE: $\overline{PL} = \text{LOW}$

Fig. 4

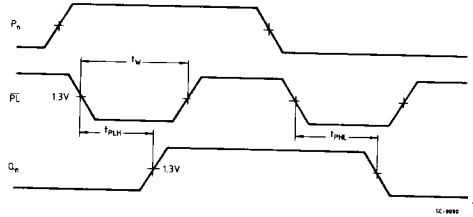


Fig. 5

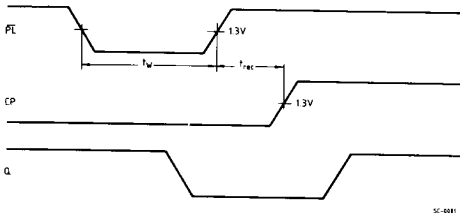


Fig. 6

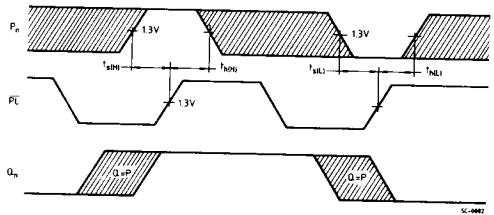
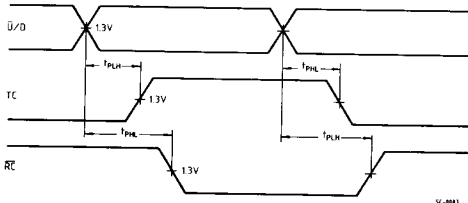


Fig. 7



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 8

