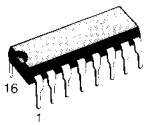
T54LS174
T74LS174

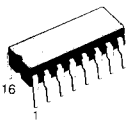
HEX D FLIP-FLOP

DESCRIPTION

The LSTTL/MSI T54LS174/T74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.
The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all SGS TTL families.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

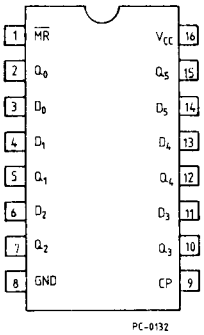
C1
Plastic Chip Carrier

ORDERING NUMBERS:
T54LS174 D2
T74LS174 D1
T74LS174 B1
T74LS174 C1
T74LS174 M1

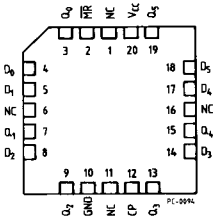
- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED-POSITIVE EDGE TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

TRUTH TABLE

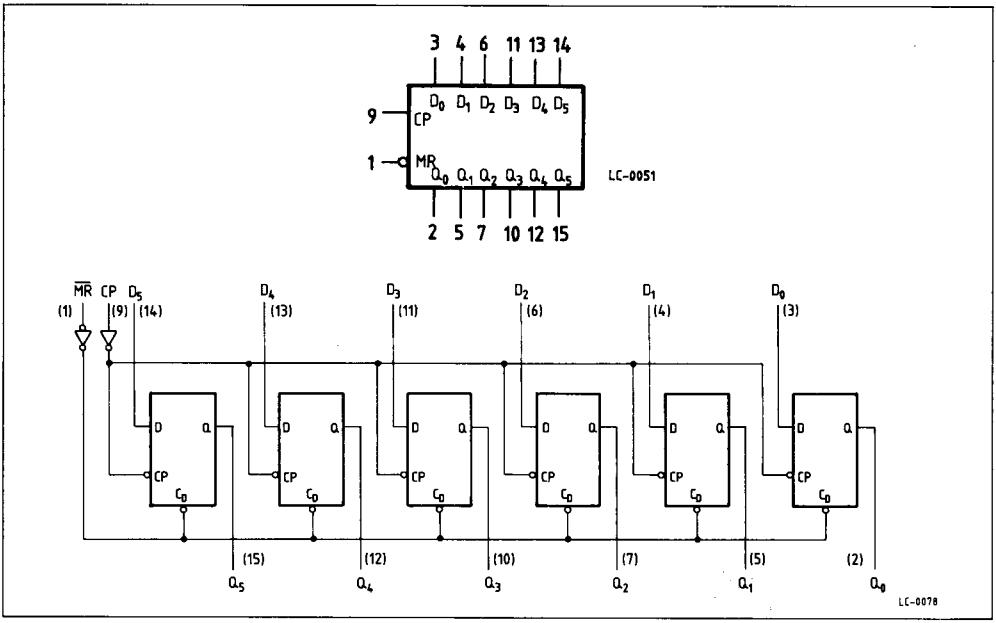
Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n + 1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

PIN NAMES

D_0-D_5	Data Input
CP	Clock (Active HIGH Going-Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0-Q_5	Outputs

LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS174D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS174XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS174 consist of six edge-triggered D flip-flop with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops.
Each D input's state is transferred to corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.
A LOW input to Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Typ.	Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Threshold Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Threshold Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA	
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA mA
I_{IL}	Input LOW Current				−0.36	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CC}	Power Supply Current			16	26	V_{CC} = MAX	mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits Min.	Typ.	Max.	Test Conditions		Units
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		20 21	30 30	Fig. 1	V_{CC} = 5.0V C_L = 15pF	ns
t_{PHL}	Propagation Delay, $\overline{MR}$ to Output		23	35	Fig. 2		ns
f_{MAX}	Maximum Input Clock Frequency	30	40		Fig. 1		MHz

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_WCP	Clock Pulse Width	20			Fig. 1		ns
t_s	Set-up Time, Data to Clock	20			Fig. 1		ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Fig. 1		ns
t_{rec}	Recovery Time for $\overline{MR}$	25			Fig. 2		ns
$t_W(\overline{MR})$	Minimum $\overline{MR}$ Pulse Width	20			Fig. 2		ns

AC WAVEFORMS

Fig. 1 Clock to Output Delays, Clock Pulse Width, Frequency Set-up and Hold Times Data to Clock

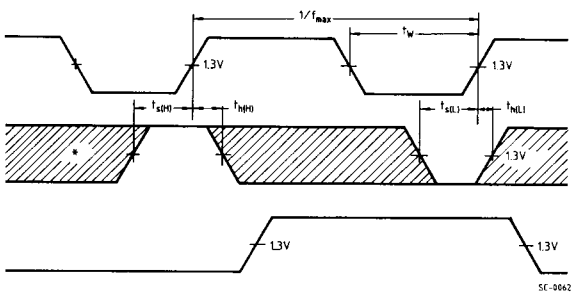
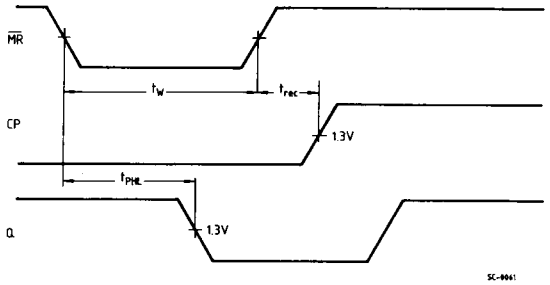


Fig. 2 Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

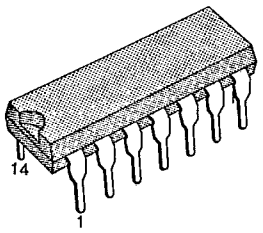


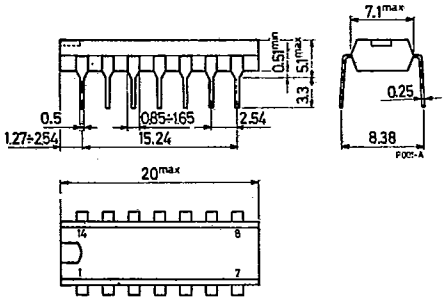
DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.
HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH at which the logic level must be mantained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transition from LOW to HIGH and still be recognized.
RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

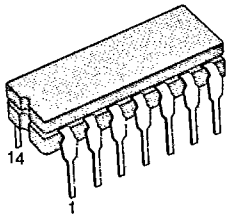
Packages

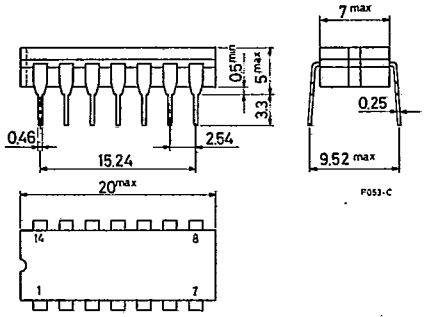
14-LEAD PLASTIC DIP





14-LEAD CERAMIC DIP





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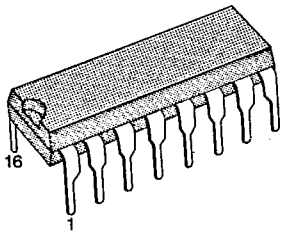
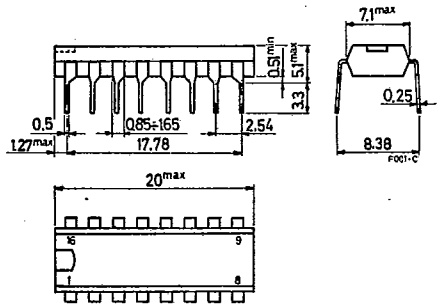
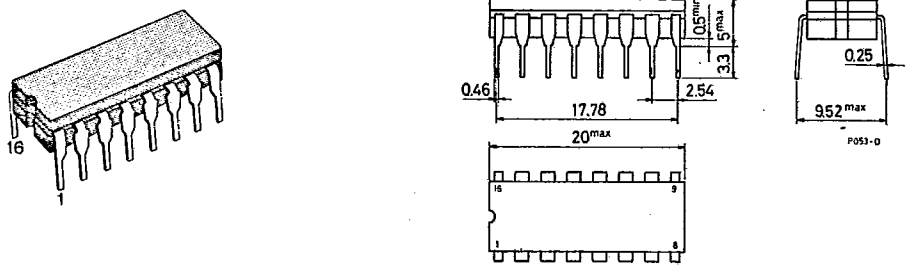




Packages

16-LEAD CERAMIC DIP



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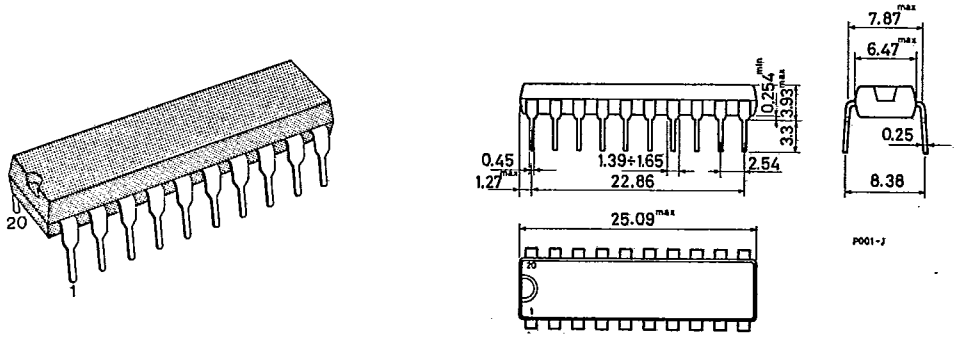

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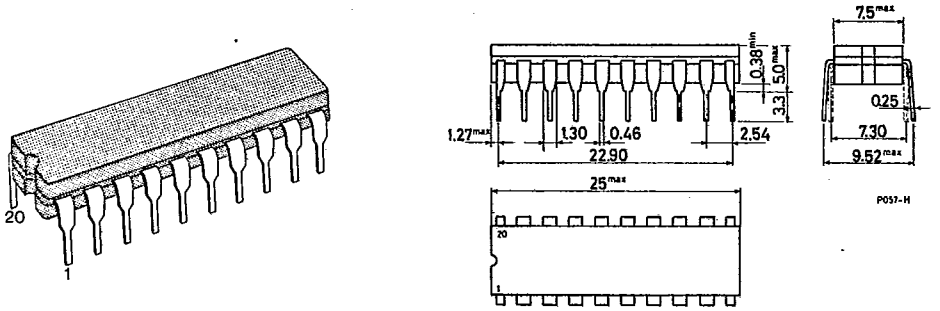
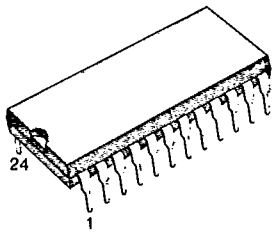
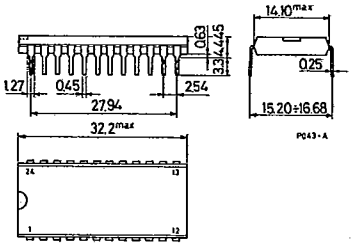


Packages

24-LEAD PLASTIC DIP





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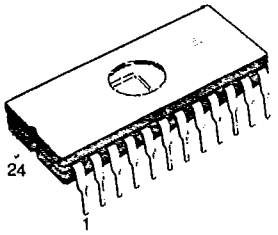
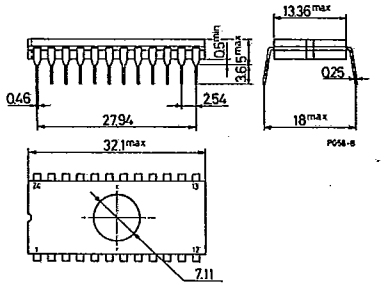
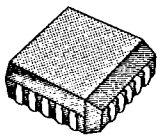
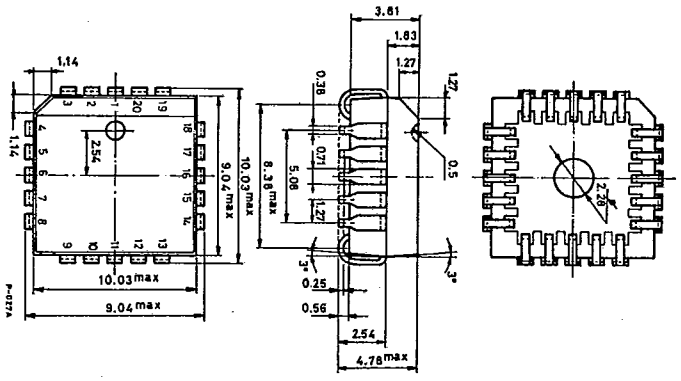




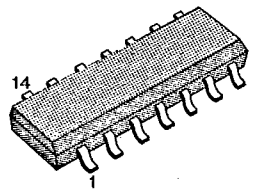
CHIP CARRIER 20 LEAD PLASTIC

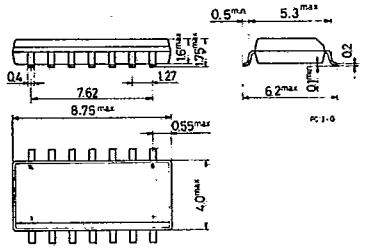




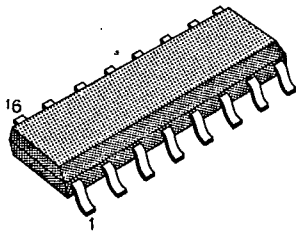
Packages

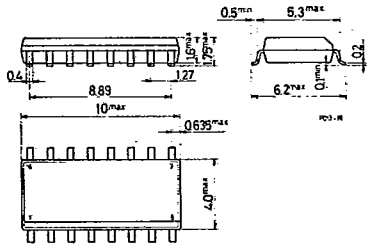
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.