



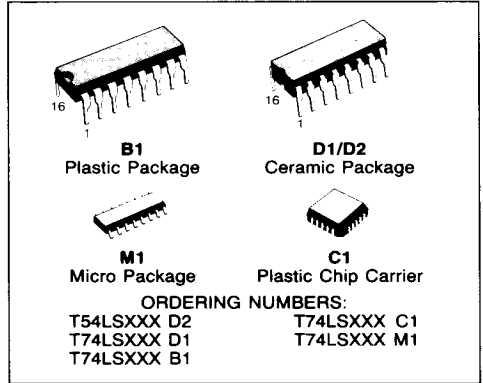
SYNCHRONOUS BI-DIRECTIONAL COUNTERS

LS168-BCD DECADE

LS169-MODULO 16 BINARY

DESCRIPTION

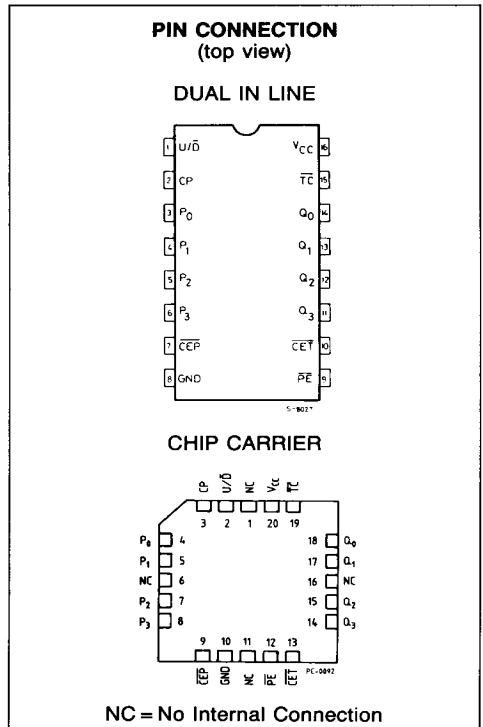
The T54LS/T74LS168 and T54LS/T74LS169 are fully synchronous 4-stage up/down counters featuring a present capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. The T54LS/T74LS168 counts in a BCD decade (8, 4, 2, 1) sequence, while the T54LS/T74LS169 operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.



- LOW POWER DISSIPATION 100mW TYPICAL
- HIGH SPEED COUNT FREQUENCY 30MHz TYPICAL
- FULLY SYNCHRONOUS OPERATION
- FULL CARRY LOOKAHEAD FOR EASY CASCADING
- SINGLE UP/DOWN CONTROL INPUT
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE
- POSITIVE EDGE-TRIGGER OPERATION

PIN NAMES

\overline{CEP}	Count Enable Parallel (Active LOW) Input
\overline{CET}	Count Enable Trickle (Active LOW) Input
CP	Clock Pulse (Active positive going edge) Input
\overline{PE}	Parallel Enable (Active LOW) Input
U/D	Up-Down Count Control Input
P ₀ -P ₃	Parallel Data Inputs
Q ₀ -Q ₃	Flip-Flop Outputs
\overline{TC}	Terminal Count (Active LOW) Output





MODE SELECT TABLE

PE	CEP	CET	U/D	Action on Rising Clock Edge
L	X	X	X	Load (Pn \rightarrow Qn)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to 7	V
V _I	Input Voltage, Applied to Input	-0.5 to 15	V
V _O	Output Voltage, Applied to Output	-0.5 to 10	V
I _I	Input Current, Into Inputs	-30 to 5	mA
I _O	Output Current, Into Outputs	50	mA

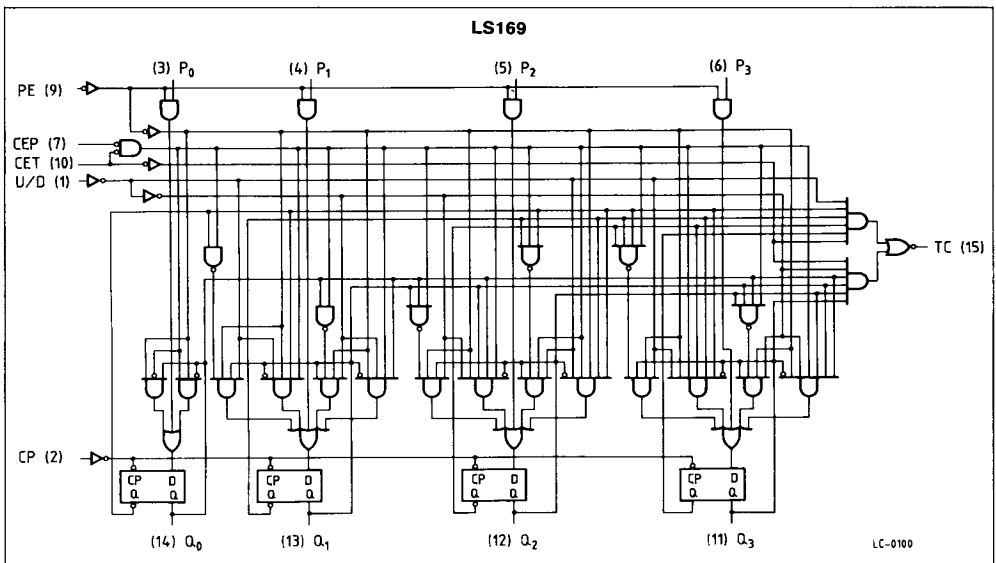
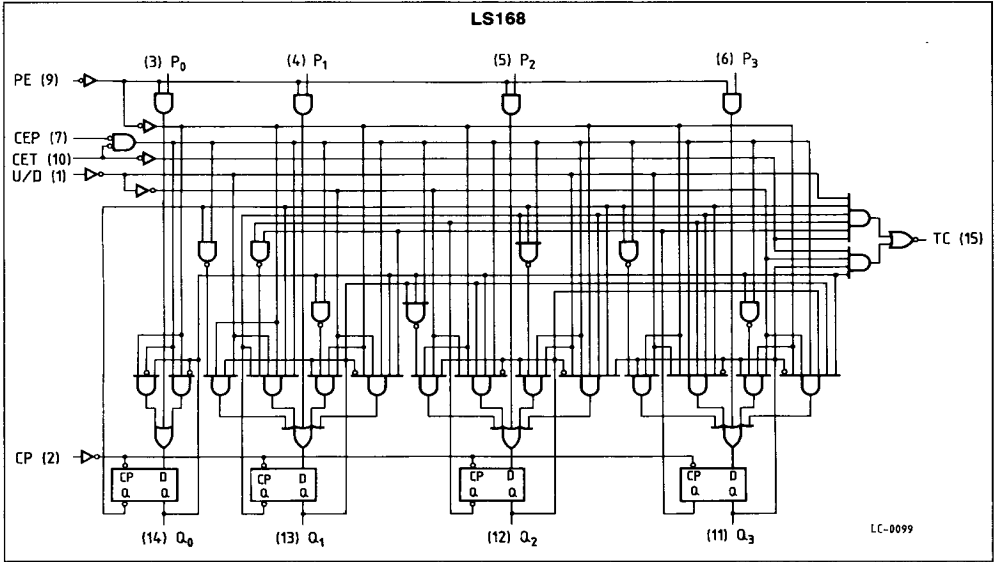
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

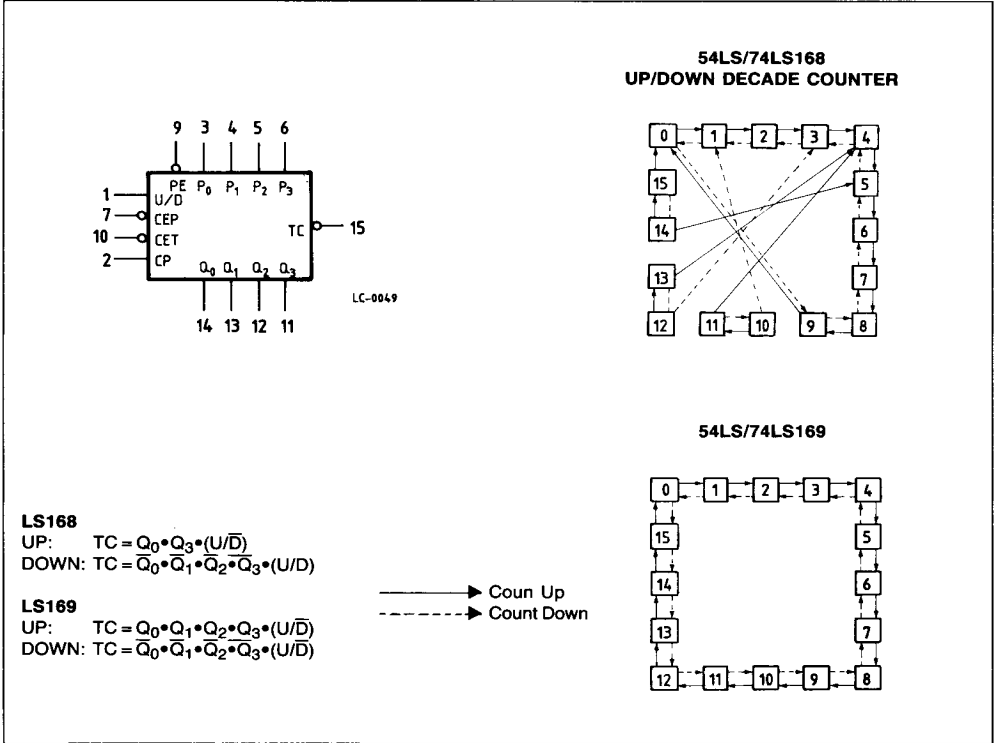
Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS168/169D2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS168/169XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

LOGIC DIAGRAMS



LOGIC SYMBOL AND STATE DIAGRAMS



FUNCTIONAL DESCRIPTION

The LS168 and LS169 use edge-triggered D-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operation, as indicated in the Mode Select Table. When \overline{PE} is LOW, the data on the P_0 - P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both \overline{CEP} and \overline{CET} must be LOW and \overline{PE} must be HIGH. The U/D input then determines the direction of counting.

The terminal count (\overline{TC}) output is normally HIGH and goes LOW, provided that \overline{CET} is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 15 (9 for the T54LS/T74LS168) in the COUNT UP mode. The TC output state is not a function of the Count Enable Parallel (\overline{CEP}) input level. The \overline{TC} output of the LS168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the LS168 will return to the legitimate sequence within two counts. Since the TC signal is derived by decoding the flip-flop states, there exist the possibility of decoding to spikes on TC. For this reason the use of \overline{TC} as a clock signal is not recommended.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

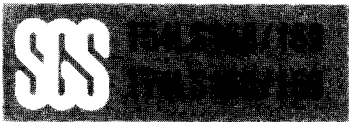
Symbol	Parameter		Limits			Test Conditions (Note 1)	Units	
			Min.	Typ.	Max.			
V _{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V	
V _{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V	
		74			0.8			
V _{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V _{CC} = MIN, I _{IN} = - 18mA	V	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V _{CC} = MIN, I _{OH} = - 400µA, V _{IN} = V _{IH} or V _{IL} per Truth Table	V	
		74	2.7	3.5				
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	I _{OL} = 4.0mA I _{OL} = 8.0mA	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table	V
		74		0.35	0.5			
I _{IH}	Input HIGH Current U/D, CP, CEP, P ₀ -P ₃ , PE CET				20 40	V _{CC} = MAX, V _{IN} = 2.7V	µA	
	U/D, CP, CEP, P ₀ -P ₃ , PE CET				0.4 0.2	V _{CC} = MAX, V _{IN} = 7.0V	mA	
I _{IL}	Input LOW Current U/D, CP, CEP, P ₀ -P ₃ , PE CET				- 0.4 - 0.8	V _{CC} = MAX, V _{IN} = 0.4V	mA	
I _{OS}	Output Short Circuit Current (Note 2)		- 20		- 100	V _{CC} = MAX, V _{OUT} = 0V	mA	
I _{CC}	Power Supply Current			20	34	V _{CC} = MAX	mA	

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter		Limits			Test Conditions	Units	
			Min.	Typ.	Max.			
t _{PLH} t _{PHL}	CP to Q			15 15	20 20	V _{CC} = 5.0V C _L = 15pF	ns	
t _{PLH} t _{PHL}	CP to TC			22 22	30 30			ns
t _{PLH} t _{PHL}	CET to TC			10 15	15 20		ns	
t _{PLH} t _{PHL}	U/D to TC			20 20	25 25			ns
f _{MAX}	Maximum Clock Frequency		25	32			Fig. 1	

Notes:

- 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at V_{CC} = 5.0V, T_A = 25°C



AC SET-UP REQUIREMENTS: $T_A = 25^\circ\text{C}$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
$t_s(L)$	Set-Up LOW, Data to CP	15	12		Fig. 4	$V_{CC} = 5.0V$
$t_s(H)$	Set-Up HIGH, Data to CP	15	12			
$t_h(L)$	Hold LOW, Data to CP	5.0	0		Fig. 4	
$t_h(H)$	Hold HIGH, Data to CP	5.0	0			
$t_s(L)$	Set-Up LOW, \overline{PE} to CP	15	12		Fig. 5	
$t_s(H)$	Set-Up HIGH, \overline{PE} to CP	15	12			
$t_h(L)$	Hold LOW, \overline{PE} to CP	5.0	0		Fig. 5	
$t_h(H)$	Hold HIGH, \overline{PE} to CP	5.0	0			
$t_s(L)$	Set-Up LOW, \overline{CET} or \overline{CEP} to CP	15	12		Fig. 5	
$t_s(H)$	Set-Up HIGH, \overline{CET} or \overline{CEP} to CP	15	12			
$t_h(L)$	Hold LOW, \overline{CET} or \overline{CEP} to CP	15	12		Fig. 5	
$t_h(H)$	Hold HIGH, \overline{CET} or \overline{CEP} to CP	15	12			
$t_s(L)$	Set-Up LOW, U/\overline{D} to CP	25	20		Fig. 6	
$t_s(H)$	Set-Up HIGH, U/\overline{D} to CP	25	20			
$t_h(L)$	Hold LOW, U/\overline{D} to CP	0	-4.0		Fig. 6	
$t_h(H)$	Hold HIGH, U/\overline{D} to CP	0	-4.0			
$t_{WCP(L)}$	Clock Pulse Width LOW	20	18		Fig. 1	
$t_{WCP(H)}$	Clock Pulse Width HIGH	10	5.0			

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS

Fig. 1 Clock to Output Delays, Count Frequency, and Clock Pulse Width

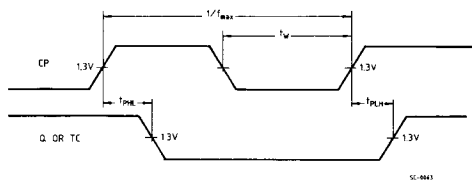
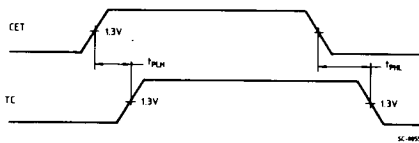


Fig. 2 Count Enable Trickle Input to Terminal Count Output Delays





AC WAVEFORMS (continued)

Fig. 3 Clock to Terminal Delays

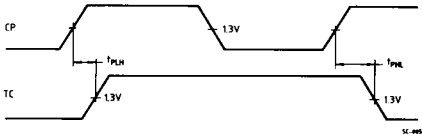


Fig. 4 Set-Up Time (t_s) and Hold (t_h) for Parallel Data Inputs

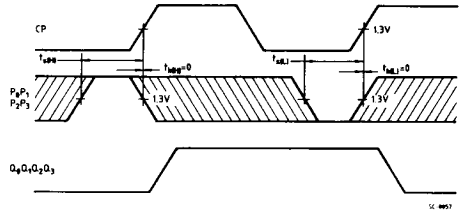
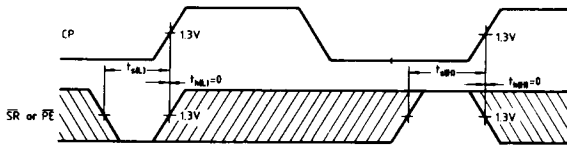
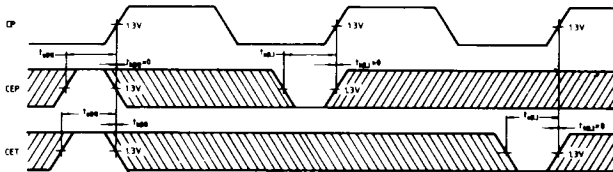


Fig. 5 Set-Up time (t_s) and hold time (t_h) for count enable (CEP) and (CET), parallel enable (PE) inputs, and up-down (U/D) control inputs.



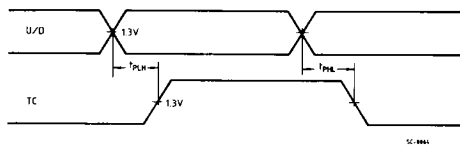
The shaded areas indicate when the input is permitted to change for predictable output performance

SC-0058A



SC-0059B

Fig. 6 Up-Down input to Terminal Count Output Delays



SC-0060