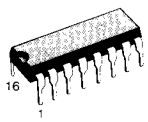
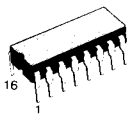
LS160/160A/162/162A: BCD DECADE COUNTERS
LS161/161A/163/163A: 4-BIT BINARY COUNTERS



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

T54LSXXXX D2
T74LSXXXX D1
T74LSXXXX B1
T74LSXXXX C1
T74LSXXXX M1

DESCRIPTION

The LS160/160A/161/161A/162/162A/163/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building, blocks for counting, memory addressing, frequency division and other applications. The LS160 and LS162 count modulo 10 (BCD). The LS161 and LS163 count modulo 16 (binary).

The LS160/160A and LS161/161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162/162A and LA163/163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

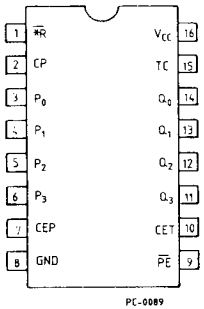
- SYNCHRONOUS COUNTING AND LOADING
- TWO COUNT ENABLE INPUTS FOR HIGH-SPEED SYNCHRONOUSLY EXPANSION
- EDGE-TRIGGERED OPERATION
- TYPICAL COUNT RATE OF 35 MHz
- FULLY TTL AND CMOS COMPATIBLE
- VERSION "A" PRELIMINARY DATA

	BCD Modulo 10	Binary (Modulo 16)
Asynchronous Reset	LS160/160A	LS161/161A
Synchronous Reset	LS162/162A	LS163/163A

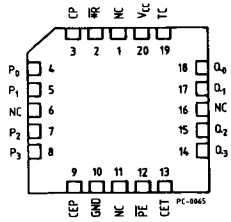
PIN NAMES

$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0-P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$\overline{SR}$	Synchronous Reset (Active LOW) Input
Q_0-Q_3	Parallel Outputs
TC	Terminal Count Output

PIN CONNECTION
(top view)
DUAL IN LINE



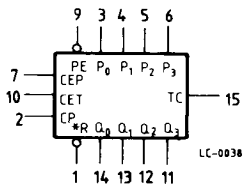
CHIP CARRIER



* $\overline{MR}$ for LS160/160A/161/161A
* $\overline{SR}$ for LS162/162A/163/163A
NC = No Internal Connection

LOGIC SYMBOL AND TRUTH TABLE

* $\overline{MR}$ for LS160/160A/161/161A
* $\overline{SR}$ for LS162/162A/163A



*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (↑)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

* For the LS162/162A and LS163/163A only

V_{CC} = Pin 16
GND = Pin 8

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS160/161/162/163D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS160/161/162/163XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS160/160A/161/161A/162/162A/163/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. These counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160/160A and LS161/161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs - Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) - select the mode of operation as shown in the tables. The Count Mode is enabled when the CEP, CET, and $\overline{PE}$ inputs are HIGH.

When the $\overline{PE}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET inputs can be used to inhibit the count sequence. With the PE held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET-CEP) allows synchronous cascading without external gating and without delay accumulation over any pratical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

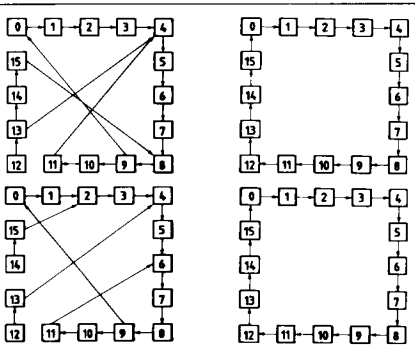
The LS160/160A and LS162/162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do not generated a TC output.

The LS161/161A and LS163/163A count modulo 16 following a binary sequence. They generated a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the LS160/160A and LS161/161A is asynchronous. When the $\overline{MR}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{MR}$ pin should never be left open. If not used, the $\overline{MR}$ pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{SR}$) input of the LS162/162A and LS163/163A acts as an edge-triggered control input, overriding CET, CEP and $\overline{PE}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g. to reset the counter synchronously after reaching a predetermined value.

STATE DIAGRAMS



LOGIC EQUATIONS

Count Enable = CEP•CET•PE
TC for LS160 & LS162 = CET•Q_0•$\overline{Q_1}$•$\overline{Q_2}$•Q_3
TC for LS161 & LS163 = CET•Q_0•Q_1•Q_2•Q_3
Preset = $\overline{PE}$•CP + (rising clock edge)
Reset = $\overline{MR}$ (LS160 & LS161)
Reset = $\overline{SR}$•CP + (rising clock edge) (LS162 & LS163)

LOGIC EQUATIONS

Count Enable = CEP•CET•PE
TC for LS160A & LS162A = CET•Q_0•$\overline{Q_1}$•$\overline{Q_2}$•Q_3
TC for LS161A & LS163A = CET•Q_0•Q_1•Q_2•Q_3
Preset = $\overline{PE}$•CP + (rising clock edge)
Reset = $\overline{MR}$ (LS160A & LS161A)
Reset = $\overline{SR}$•CP + (rising clock edge (LS162A & LS163A)

NOTE: The LS160/160A and LS162/162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (LS160/161/162/163).

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
I_{IH}	Input HIGH Current P_0-P_3, $\overline{MR}$, $\overline{SR}$				20	V_{CC} = MAX, V_{IN} = 2.7V	μA
	$\overline{PE}$, CEP, CP				24		
	CET				40		
	P_0-P_3, $\overline{MR}$, $\overline{SR}$, $\overline{PE}$, CEP, CP				0.1	V_{CC} = MAX, V_{IN} = 7.0V	mA
	CET				0.2		
I_{IL}	Input LOW Current P_0-P_3, $\overline{MR}$, $\overline{SR}$				−0.40	V_{CC} = MAX, V_{IN} = 0.4V	mA
	$\overline{PE}$, CEP, CP				−0.48		
	CET				−0.80		
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CCH}	Power Supply Current			18	31	V_{CC} = MAX	mA
I_{CCL}				19	32		

AC CHARACTERISTICS: T_A = 25°C (LS160/161/162/163)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions		Units
t_{PLH}	Turn Off Delay CP to Q		13	25	Fig. 1	V_{CC} = 5.0V, C_L = 15pF	ns
t_{PHL}	Turn On Delay CP to Q		18	27			
t_{PLH}	Turn Off Delay CP to TC		15	25	Fig. 4		ns
t_{PHL}	Turn On Delay CP to TC		14	21			
t_{PLH}	Turn Off Delay CET to TC		9.0	14	Fig. 3		ns
t_{PHL}	Turn On Delay CET to TC		16	23			
t_{PHL}	Turn On Delay $\overline{MR}$ to Q (LS160 and LS161 only)		18	28	Fig. 2		ns
f_{count}	Input Count Frequency	25	35		Fig. 1		MHz

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: $T_A = 25°C$ (LS160/161/162/163)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{rec}	Recovery Time for $\overline{MR}$ (LS160 and LS161 Only)	20			Fig. 1	$V_{CC} = 5.0V$	ns
$t_W MR(L)$	Master Reset Pulse width (LS160 and LS161 Only)	15			Fig. 2		ns
$t_W CP(H)$	Clock Pulse Width (HIGH)	15			Fig. 1		ns
$t_W CP(L)$	Clock Pulse Width (LOW)	25					
$t_s(H)$	Set-up Time (HIGH), Data to Clock	20			Fig. 5		ns
$t_s(L)$	Set-up Time (LOW), Data to Clock	20					
$t_h(H)$	Hold Time (HIGH), Data to Clock	3.0					ns
$t_h(L)$	Hold Time (LOW), Data to Clock	3.0					
$t_s(H)$	Set-up Time (HIGH), $\overline{PE}$ or $\overline{SR}$ to Clock	25			Fig. 6		ns
$t_s(L)$	Set-up Time (LOW), $\overline{PE}$ or $\overline{SR}$ to Clock	25					
$t_h(H)$	Hold Time (HIGH), $\overline{PE}$ or $\overline{SR}$ to Clock	0					ns
$t_h(L)$	Hold Time (LOW), $\overline{PE}$ or $\overline{SR}$ to Clock	0					
$t_s(H)$	Set-up Time (HIGH), CE to Clock	25			Fig. 7		ns
$t_s(L)$	Set-up Time (LOW), CE to Clock	25					
$t_h(H)$	Hold Time (HIGH), CE to Clock	0					ns
$t_h(L)$	Hold Time (LOW), CE to Clock	0					

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) - is defined as the minimim time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (LS160A/161A/162A/163A).

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.5			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA	
I_{IH}	Input HIGH Current $\overline{MR}$, Data, CEP, Clock $\overline{PE}$, CET (LS160A/161A)				20 40	V_{CC} = MAX, V_{IN} = 2.7V	μA
	$\overline{MR}$, Data, CEP, Clock $\overline{PE}$, CET (LS160A/161A)				0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0V	mA
I_{IH}	Input HIGH Current Data, CEP, Clock $\overline{PE}$, CET, $\overline{SR}$ (LS160A/161A)				20 40	V_{CC} = MAX, V_{IN} = 2.7V	μA
	Data, CEP, Clock $\overline{PE}$, CET, $\overline{SR}$ (LS162A/163A)				0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0V	mA
I_{IL}	Input LOW Current $\overline{MR}$, Data, CEP, Clock $\overline{PE}$, CET (LS160A/161A)				−0.4 −0.8	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{IL}	Input LOW Current Data, CEP, Clock $\overline{PE}$, CET, $\overline{SR}$ (LS162A/163A)				−0.4 −0.8	V_{CC} = MAX, V_{IN} = 0.4V	μA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CCH} I_{CCL}	Power Supply Current			18 19	31 32	V_{CC} = MAX	mA

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS: $T_A = 25°C$ (LS160A/161A/162A/163A)

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Clock to TC		20 18	35 35	$V_{CC} = 5.0V$ $C_L = 15pF$	ns
t_{PLH} t_{PHL}	Propagation Delay, Clock to Q		13 18	24 27		ns
t_{PLH} t_{PHL}	Propagation Delay, CET to TC		9.0 9.0	14 14		ns
t_{PHL}	$\overline{MR}$ or $\overline{SR}$ to Q		20	28		ns
f_{MAX}	Maximum Clock Frequency	25	32			MHz

AC CHARACTERISTICS: $T_A = 25°C$ (LS160A/161A/162A/163A)

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_WCP	Clock Pulse Width	25			$V_{CC} = 5.0V$	ns
t_W	$\overline{MR}$ or SR Pulse Width	20				ns
t_s	Set-up Time, Any Input	20				ns
t_h	Hold Time, Any Input	0				ns

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) - is defined as the minimim time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognized and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

Fig. 1 Clock to Output Delays, Count Frequency, and Clock Pulse Width

Other Conditions:
$\overline{PE} = \overline{MR}\ (\overline{SR}) = H$ $\quad CEP = CET = H$

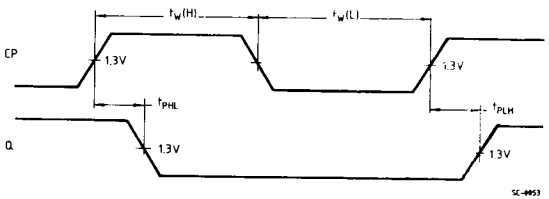


Fig. 2 Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

Other Conditions: $\overline{PE} = L$
$P_0 = P_1 = P_2 = P_3 = H$

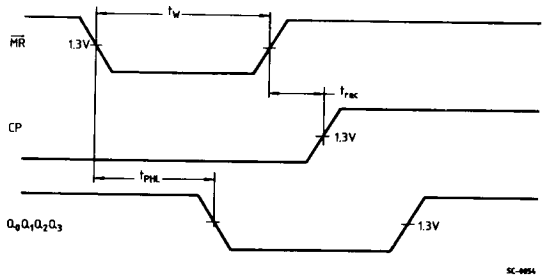


Fig. 3 Count Enable Trickle Input to Terminal Count Output Delays

The positive TC pulse occurs when the outputs are in the $(Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3)$ state for the LS160/160A and LS162/162A and the $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ state for the LS161/161A and LS163/163A.

Other Conditions:
$CP = \overline{PE} = CEP = \overline{MR} = H$

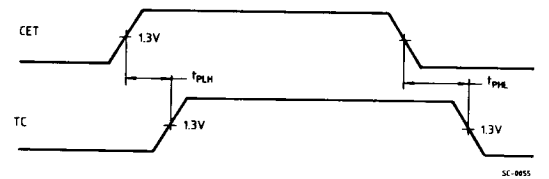
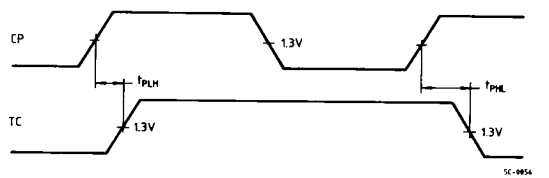


Fig. 4 Clock to Terminal Count Delays

The positive TC pulse in coincident with the output state $(Q_0 \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet Q_3)$ for the LS160/160A and LS162/162A and $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$ state for the LS161/161A and LS163/163A.

Other Conditions:
$\overline{PE} = CEP = CET = \overline{MR} = H$



AC WAVEFORMS (Continued)

Fig. 5 Set-up Time (t_s) and Hold Time (t_h) for Parallel Data Inputs.

Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H

The shaded areas indicate when the input is permitted to change for predictable output performance.

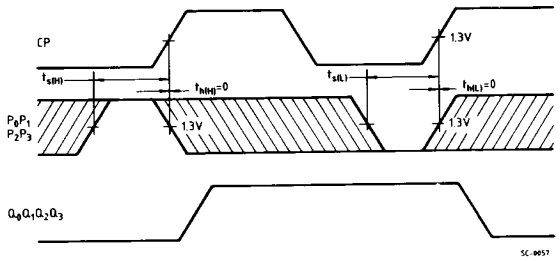


Fig. 6 Set-up Time (t_s) and Hold Time (t_h) for Count Enable (CEP) and (CET) and Parallel Enable ($\overline{PE}$) Inputs.

Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H

The shaded areas indicate when the input is permitted to change for predictable output performance.

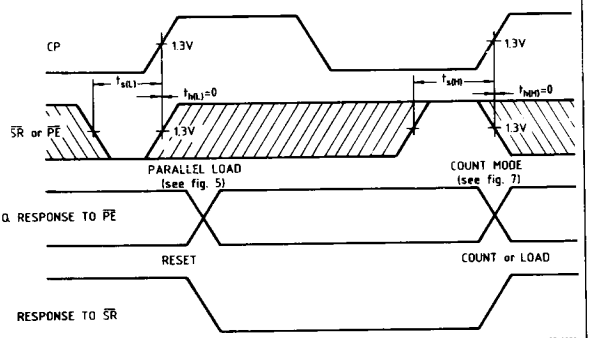


Fig. 7

Other Conditions: $\overline{PE}$ = H, $\overline{MR}$ = H