

T54LS158
T74LS158



QUAD 2-INPUT MULTIPLEXER

DESCRIPTION

The TTL/MSI T54LS158/T74LS158 is a high speed Quad 2-Input Multiplexer. It selects four bits of data from two sources using common Select and Enable inputs. The four buffered outputs present the selected data in the true inverted form. The LS158 can also generate any four of the 16 different functions of two variables. The LS158 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all SGS TTL families.

B1
Plastic Package

D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
 T54LS158 D2 T74LS158 C1
 T74LS158 D1 T74LS158 M1
 T74LS158 B1

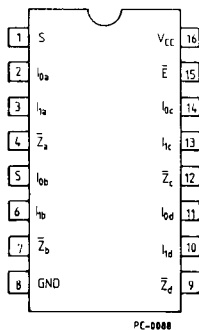
- SCHOTTKY PROCESS FOR HIGH SPEED
- MULTIFUNCTION CAPABILITY
- INVERTING OUTPUTS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

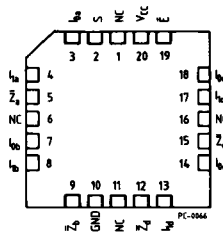
S	Common Select Input
\bar{E}	Enable (Active LOW) Input
$1a-1d$	Data Inputs from Source 0
$1a-1d$	Data Inputs from Source 1
$Za-Zd$	Inverted Outputs

PIN CONNECTION (top view)

DUAL IN LINE



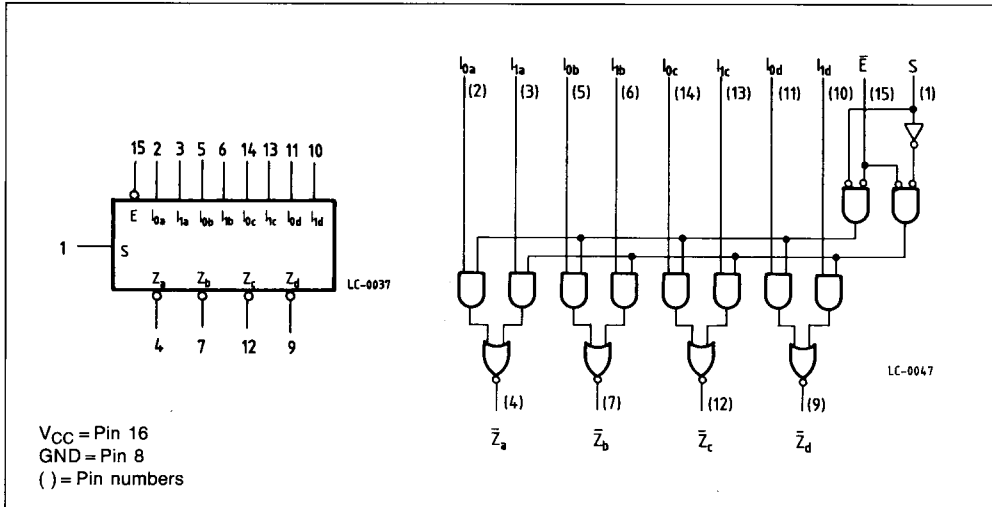
CHIP CARRIER



NC = No Internal Connection



LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	Input Voltage, Applied to Input	-0.5 to 15	V
V_O	Output Voltage, Applied to Output	-0.6 to 10	V
I_I	Input Current, Into Inputs	-30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS158D2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS158XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.



FUNCTIONAL DESCRIPTION

The LS158 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of the common Select Input (S) and present the data in inverted form at the four outputs. The Enable Input (\bar{E}) is active LOW. When \bar{E} is HIGH, all of the outputs (\bar{Z}) are forced HIGH regardless of all other inputs.

The LS158 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels supplied to the Select Inputs.

A common use of the LS158 is the moving of data from two groups of registers to four common output buses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
\bar{E}	S	I_0	I_1	\bar{Z}
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

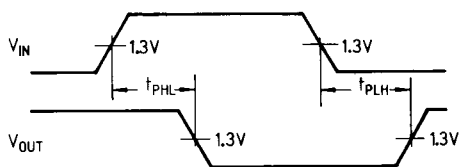
H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

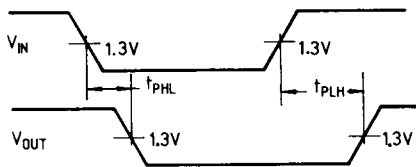
AC WAVEFORMS

Fig. 1

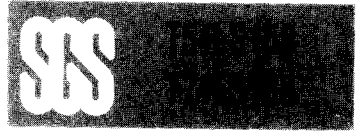


SC-0009

Fig. 2



SC-0007



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units	
			Min.	Typ.	Max.			
V _{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V	
V _{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V	
		74			0.8			
V _{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V _{CC} = MIN, I _{IN} = -18mA	V	
V _{OH}	Output HIGH Voltage	54	2.5	3.4		V _{CC} = MIN, I _{OH} = -400μA, V _{IN} = V _{IH} or V _{IL} per Truth Table	V	
		74	2.7	3.4				
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	I _{OL} = 4.0mA I _{OL} = 8.0mA	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table	V
		74		0.35	0.5			
I _{IH}	Input HIGH Current I ₀ , I ₁ E, S				20 40	V _{CC} = MAX, V _{IN} = 2.7V	μA	
	Input HIGH Current at Max Input Voltage I ₀ , I ₁ E, S				0.1 0.2	V _{CC} = MAX, V _{IN} = 7.0V	mA	
I _{IL}	Input LOW Current I ₀ , I ₁ E, S				-0.4 -0.8	V _{CC} = MAX, V _{IN} = 0.4V	mA	
I _{OS}	Output Short Circuit Current (Note 2)		-20		-100	V _{CC} = MAX, V _{OUT} = 0V	mA	
I _{CC}	Power Supply Current			5.0	8.0	V _{CC} = MAX	mA	

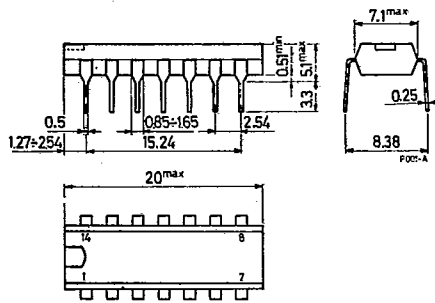
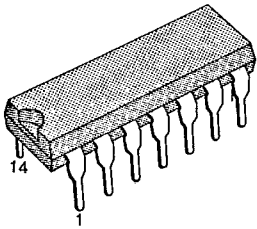
AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter		Limits			Test Conditions	Units	
			Min.	Typ.	Max.			
t _{PLH} t _{PHL}	Propagation Delay, Select to Output			13 16	20 24	Fig. 1 Fig. 2 Fig. 1	V _{CC} = 5.0V C _L = 15pF	ns
t _{PLH} t _{PHL}	Propagation Delay, Enable to Output			11 18	17 24			
t _{PLH} t _{PHL}	Propagation Delay, Data to Output			7 10	12 15			

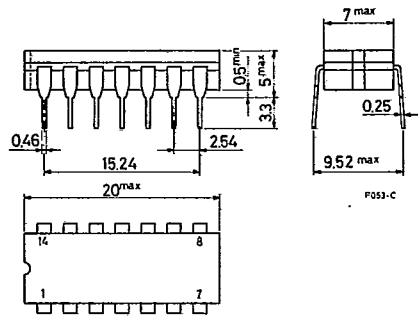
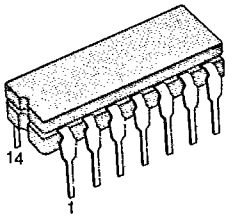
Notes:

- 1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

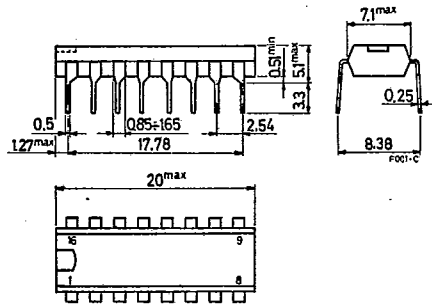
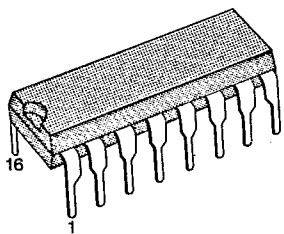
14-LEAD PLASTIC DIP



14-LEAD CERAMIC DIP



16-LEAD PLASTIC DIP



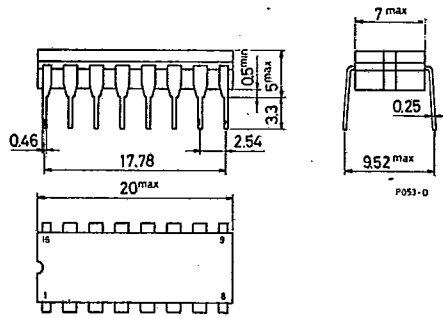
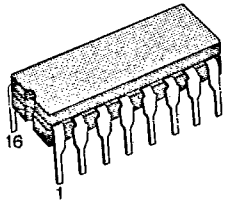
Packages

67C 16545

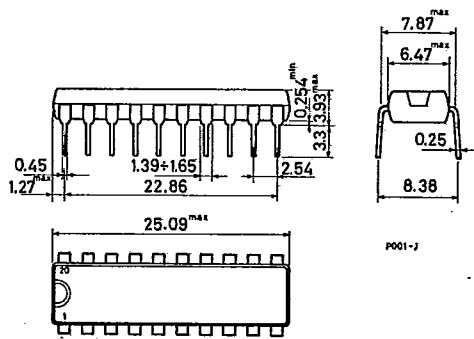
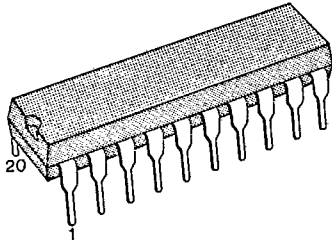
D

T-90-20

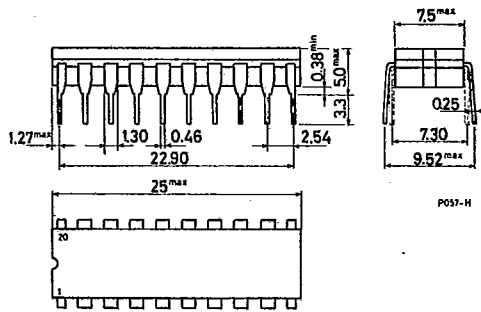
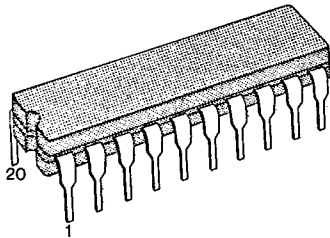
16-LEAD CERAMIC DIP



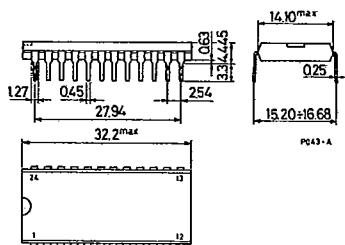
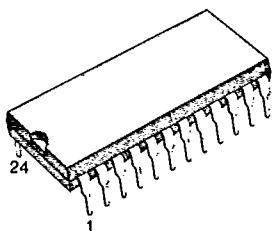
20-LEAD PLASTIC DIP



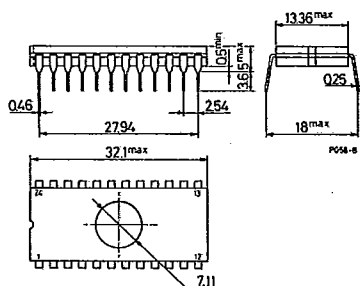
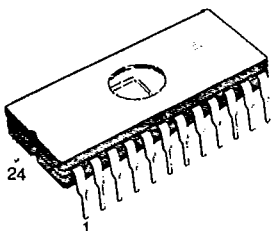
20-LEAD CERAMIC DIP



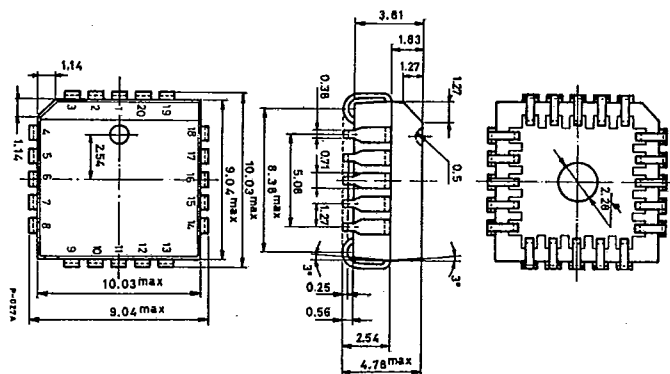
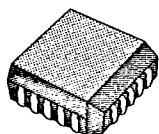
24-LEAD PLASTIC DIP



24-LEAD CERAMIC DIP



CHIP CARRIER 20 LEAD PLASTIC



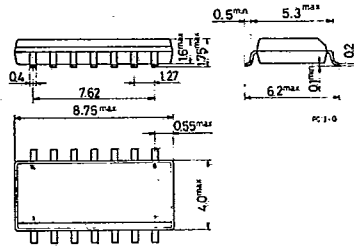
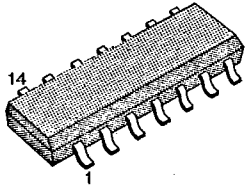
Packages

67C 16547

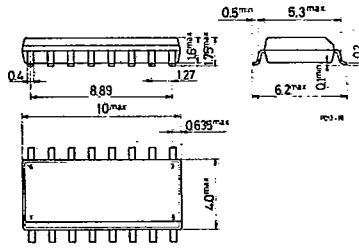
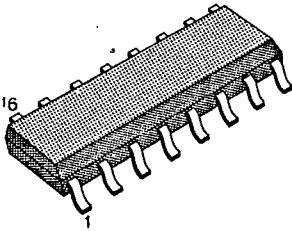
D

T-90-20

14-LEAD PLASTIC DIP MICROPACKAGE



16-LEAD PLASTIC DIP MICROPACKAGE



NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

67C 16548

D

T-90-20

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages. The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propagation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.

