



OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES

| | |
|--------------------------------|--------------------------------------|
| D ₀ -D ₇ | Data Inputs |
| LE | Latch Enable (Active HIGH) Input |
| CP | Clock (Active HIGH going edge) Input |
| OE | Output Enable (Active LOW) Input |
| O ₀ -O ₇ | Outputs (Note b) |

| LOADING (Note a) | |
|------------------|---------------|
| HIGH | LOW |
| 0.5 U.L. | 0.25 U.L. |
| 0.5 U.L. | 0.25 U.L. |
| 0.5 U.L. | 0.25 U.L. |
| 0.5 U.L. | 0.25 U.L. |
| 65 (25) U.L. | 15 (7.5) U.L. |

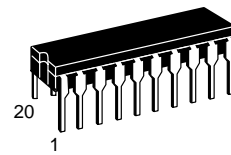
NOTES:

- a) 1 TTL Units Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

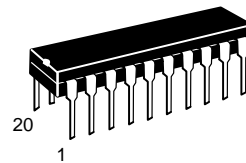
SN54/74LS373
SN54/74LS374

**OCTAL TRANSPARENT LATCH
WITH 3-STATE OUTPUTS;
OCTAL D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUT**

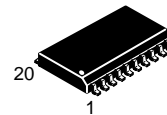
LOW POWER SCHOTTKY



**J SUFFIX
CERAMIC
CASE 732-03**



**N SUFFIX
PLASTIC
CASE 738-03**



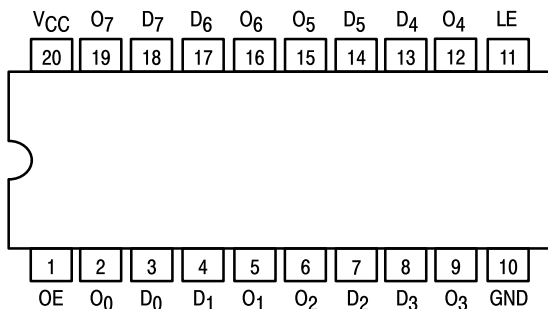
**DW SUFFIX
SOIC
CASE 751D-03**

ORDERING INFORMATION

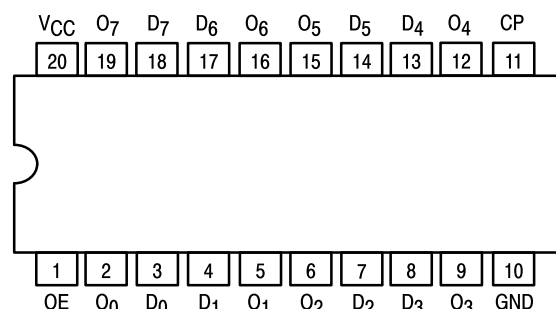
SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXDW SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)

SN54/74LS373



SN54/74LS374



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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TRUTH TABLE

LS373

| D _n | LE | OE | O _n |
|----------------|----|----|----------------|
| H | H | L | H |
| L | H | L | L |
| X | L | L | Q ₀ |
| X | X | H | Z* |

LS374

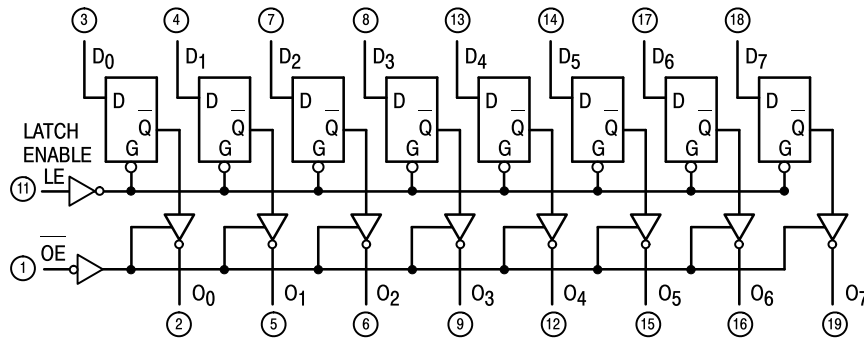
| D _n | LE | OE | O _n |
|----------------|----|----|----------------|
| H | | L | H |
| L | | L | L |
| X | X | H | Z* |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

* Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE).

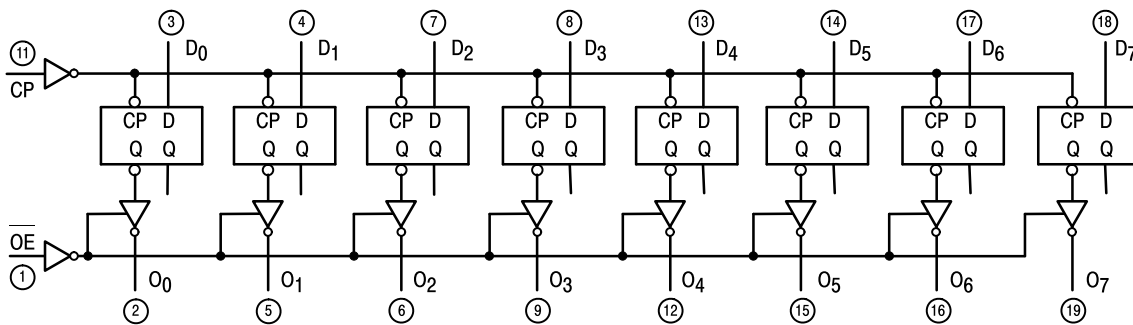
LOGIC DIAGRAMS

SN54LS/74LS373



V_{CC} = PIN 20
GND = PIN 10
○ = PIN NUMBERS

SN54LS/74LS374



GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|----|------|-----|------|------|
| V _{CC} | Supply Voltage | 54 | 4.5 | 5.0 | 5.5 | V |
| | | 74 | 4.75 | 5.0 | 5.25 | |
| T _A | Operating Ambient Temperature Range | 54 | -55 | 25 | 125 | °C |
| | | 74 | 0 | 25 | 70 | |
| I _{OH} | Output Current — High | 54 | | | -1.0 | mA |
| | | 74 | | | -2.6 | |
| I _{OL} | Output Current — Low | 54 | | | 12 | mA |
| | | 74 | | | 24 | |

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | Limits | | | Unit | Test Conditions | |
|------------------|--------------------------------|--------|-------|------|------|--|--|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| V _{IL} | Input LOW Voltage | 54 | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | 0.8 | | | |
| V _{IK} | Input Clamp Diode Voltage | | -0.65 | -1.5 | V | V _{CC} = MIN, I _{IN} = -18 mA | |
| V _{OH} | Output HIGH Voltage | 54 | 2.4 | 3.4 | V | V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table | |
| | | 74 | 2.4 | 3.1 | V | | |
| V _{OL} | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | I _{OL} = 12 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | |
| I _{OZH} | Output Off Current HIGH | | | 20 | μA | V _{CC} = MAX, V _{OUT} = 2.7 V | |
| I _{OZL} | Output Off Current LOW | | | -20 | μA | V _{CC} = MAX, V _{OUT} = 0.4 V | |
| I _{IH} | Input HIGH Current | | | 20 | μA | V _{CC} = MAX, V _{IN} = 2.7 V | |
| | | | | 0.1 | mA | V _{CC} = MAX, V _{IN} = 7.0 V | |
| I _{IL} | Input LOW Current | | | -0.4 | mA | V _{CC} = MAX, V _{IN} = 0.4 V | |
| I _{OS} | Short Circuit Current (Note 1) | -30 | | -130 | mA | V _{CC} = MAX | |
| I _{CC} | Power Supply Current | | | 40 | mA | V _{CC} = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

| Symbol | Parameter | Limits | | | | | | Unit | Test Conditions |
|--------------------------------------|--------------------------------------|--------|----------|----------|-------|----------|----------|------|---|
| | | LS373 | | | LS374 | | | | |
| | | Min | Typ | Max | Min | Typ | Max | | |
| f _{MAX} | Maximum Clock Frequency | | | | 35 | 50 | | MHz | C _L = 45 pF, R _L = 667 Ω |
| t _{PLH} t _{PHL} | Propagation Delay, Data to Output | | 12 12 | 18 18 | | | | ns | |
| t _{PLH} t _{PHL} | Clock or Enable to Output | | 20 18 | 30 30 | | 15 19 | 28 28 | ns | |
| t _{PZH} t _{PZL} | Output Enable Time | | 15 25 | 28 36 | | 20 21 | 28 28 | ns | |
| t _{PHZ} t _{PLZ} | Output Disable Time | | 12 15 | 20 25 | | 12 15 | 20 25 | ns | C _L = 5.0 pF |

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

| Symbol | Parameter | Limits | | | | Unit |
|----------------|-------------------|--------|-----|-------|-----|------|
| | | LS373 | | LS374 | | |
| | | Min | Max | Min | Max | |
| t _W | Clock Pulse Width | 15 | | 15 | | ns |
| t _S | Setup Time | 5.0 | | 20 | | ns |
| t _H | Hold Time | 20 | | 0 | | ns |

DEFINITION OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

SN54/74LS373

AC WAVEFORMS

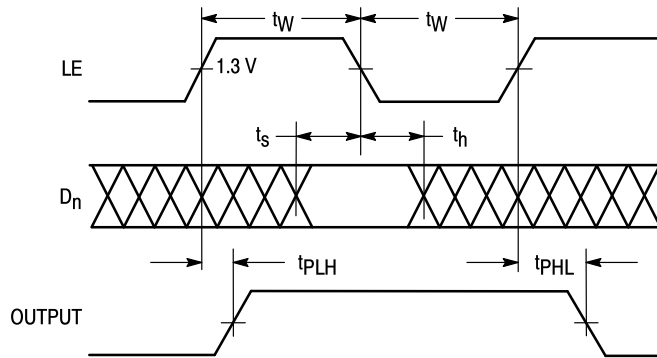


Figure 1

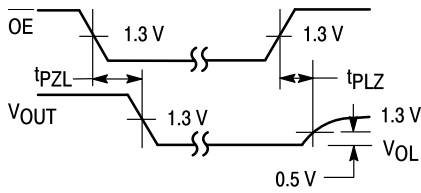


Figure 2

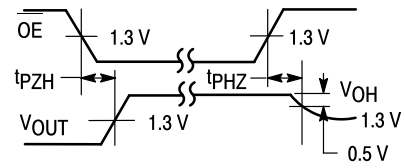
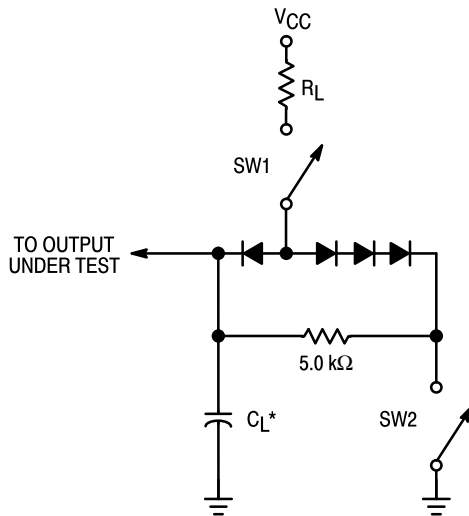


Figure 3

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 4

SWITCH POSITIONS

| SYMBOL | SW1 | SW2 |
|-----------|--------|--------|
| t_{pZH} | Open | Closed |
| t_{pZL} | Closed | Open |
| t_{pLZ} | Closed | Closed |
| t_{pHZ} | Closed | Closed |

SN54/74LS374

AC WAVEFORMS

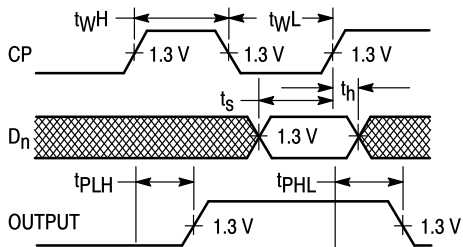


Figure 5

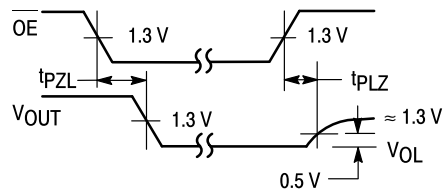


Figure 6

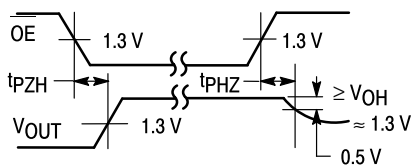
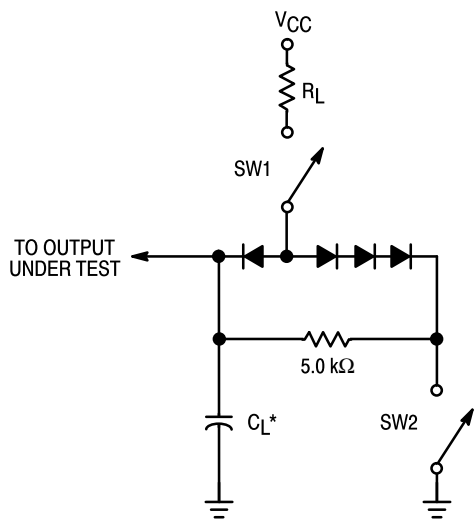


Figure 7

AC LOAD CIRCUIT



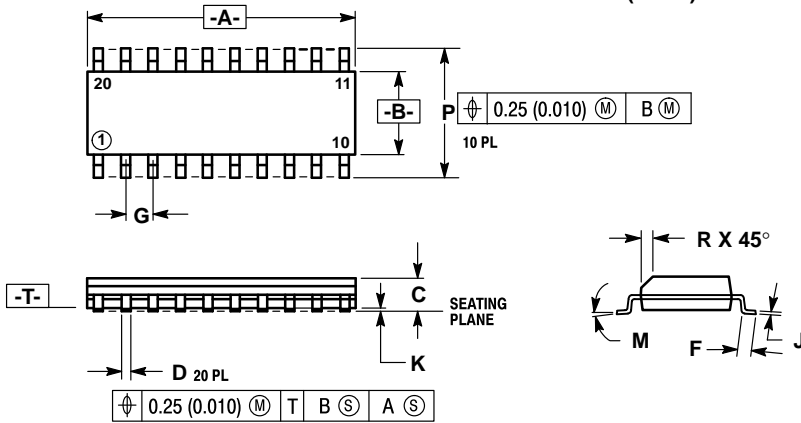
* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

| SYMBOL | SW1 | SW2 |
|--------|--------|--------|
| tPZH | Open | Closed |
| tPZL | Closed | Open |
| tPLZ | Closed | Closed |
| tPHZ | Closed | Closed |

Figure 8

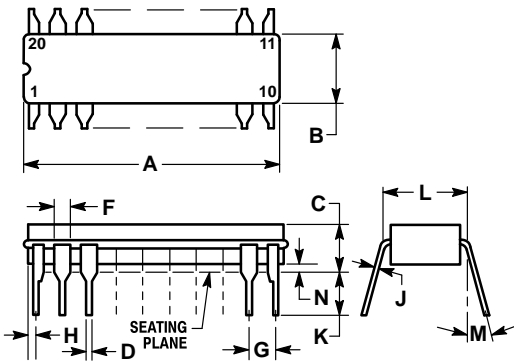
**Case 751D-03 DW Suffix
20-Pin Plastic
SO-20 (WIDE)**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 12.65 | 12.95 | 0.499 | 0.510 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

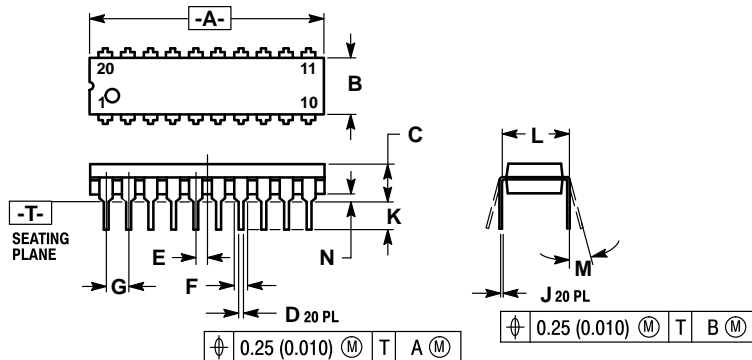
**Case 732-03 J Suffix
20-Pin Ceramic Dual In-Line**



- NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIM A AND B INCLUDES MENISCUS.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 23.88 | 25.15 | 0.940 | 0.990 |
| B | 6.60 | 7.49 | 0.260 | 0.295 |
| C | 3.81 | 5.08 | 0.150 | 0.200 |
| D | 0.38 | 0.56 | 0.015 | 0.022 |
| F | 1.40 | 1.65 | 0.055 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.51 | 1.27 | 0.020 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.25 | 1.02 | 0.010 | 0.040 |

**Case 738-03 N Suffix
20-Pin Plastic**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 5. 738-02 OBSOLETE, NEW STANDARD 738-03.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 25.66 | 27.17 | 1.010 | 1.070 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.81 | 4.57 | 0.150 | 0.180 |
| D | 0.39 | 0.55 | 0.015 | 0.022 |
| E | 1.27 BSC | | 0.050 BSC | |
| F | 1.27 | 1.77 | 0.050 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.21 | 0.38 | 0.008 | 0.015 |
| K | 2.80 | 3.55 | 0.110 | 0.140 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.01 | 0.020 | 0.040 |

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| SYMBOL | SW1 | SW2 |
|--------|--------|--------|
| tpZH | Open | Closed |
| tpZL | Closed | Open |
| tpLZ | Closed | Closed |

