



SN54LS182 SN74LS182

DESCRIPTION — The SN54LS/74LS182 is a high-speed Carry Lookahead Generator. It is generally used with the SN54LS/74LS181 4-Bit Arithmetic Logic Unit to provide high speed lookahead over word lengths of more than four bits. The carry lookahead generator is fully compatible with all members of the Motorola TTL Family.

CARRY LOOKAHEAD GENERATOR

LOW POWER SCHOTTKY

- PROVIDES CARRY LOOKAHEAD ACROSS A GROUP OF FOUR ALUs
- MULTI-LEVEL LOOKAHEAD FOR HIGH-SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

PIN NAMES

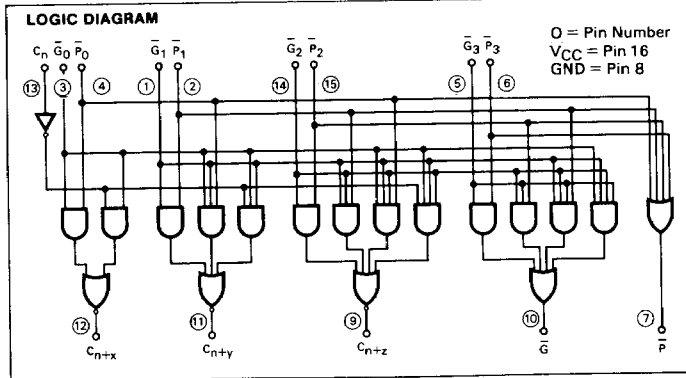
C_n	Carry Input
$\bar{G}_0, \bar{G}_1, \bar{G}_2$	Carry Generate (Active LOW) Inputs
$\bar{G}_0, \bar{G}_1, \bar{G}_2$	Carry Generate (Active LOW) Input
$\bar{G}_0, \bar{G}_1, \bar{G}_2$	Carry Generate (Active LOW) Input
\bar{P}_0, \bar{P}_1	Carry Propagate (Active LOW) Inputs
\bar{P}_0, \bar{P}_1	Carry Propagate (Active LOW) Input
\bar{P}_0, \bar{P}_1	Carry Propagate (Active LOW) Input
$C_{n+x}, C_{n+y}, C_{n+z}$	Carry Outputs (Note b)
\bar{G}	Carry Generate (Active LOW) Output (Note b)
\bar{P}	Carry Propagate (Active LOW) Output (Note b)

LOADING (Note a)

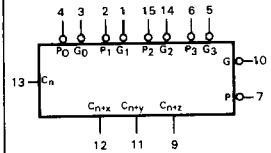
	HIGH	LOW
C_n	0.5 U.L.	0.25 U.L.
$\bar{G}_0, \bar{G}_1, \bar{G}_2$	3.5 U.L.	1.75 U.L.
\bar{P}_0, \bar{P}_1	4.0 U.L.	2.0 U.L.
$\bar{G}_0, \bar{G}_1, \bar{G}_2$	2.0 U.L.	1.0 U.L.
\bar{P}_0, \bar{P}_1	2.0 U.L.	1.0 U.L.
\bar{G}	1.5 U.L.	0.75 U.L.
\bar{P}	1.0 U.L.	0.5 U.L.
$C_{n+x}, C_{n+y}, C_{n+z}$	10 U.L.	5 (2.5) U.L.
\bar{G}	10 U.L.	5 (2.5) U.L.
\bar{P}	10 U.L.	5 (2.5) U.L.

NOTES:

- 1 Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

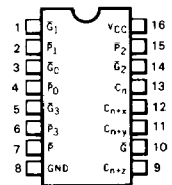


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-08 (Ceramic)
N Suffix — Case 648-05 (Plastic)

NOTE:

The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The SN54LS/74LS182, carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P_0}, \overline{P_1}, \overline{P_2}, \overline{P_3}$) and Carry Generate ($\overline{G_0}, \overline{G_1}, \overline{G_2}, \overline{G_3}$) signals and an active HIGH Carry Input (C_n) and provides anticipated active HIGH carries ($C_{n+x}, C_{n+y}, C_{n+z}$) across four groups of binary adders. The SN54LS/74LS182 also has active LOW Carry Propagate (\overline{P}) and Carry Generate (\overline{G}) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$\begin{aligned}
 C_{n+x} &= \overline{G_0} + P_0 C_n \\
 C_{n+y} &= \overline{G_1} + P_1 \overline{G_0} = P_1 P_0 C_n \\
 C_{n+z} &= \overline{G_2} + P_2 \overline{G_1} = P_2 P_2 \overline{G_0} + P_2 P_1 P_0 C_n \\
 \overline{G} &= \overline{G_3} + P_3 \overline{G_2} + P_3 P_2 \overline{G_1} + P_3 P_2 P_1 \overline{G_0} \\
 \overline{P} &= P_3 P_2 P_1 P_0
 \end{aligned}$$

Also, the SN54LS/74LS182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	C_{n+x}	C_{n+y}	C_{n+z}	\overline{G}	\overline{P}
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
X			X	X	X	X	H	H				H	
X			X	X	H	H	H	X				H	
X			H	H	H	X	H	X				H	
H			H	X	H	X	H	X				H	
X			X	X	X	X	L	X				L	
X			X	X	L	X	X	L				L	
X			L	X	X	L	X	L				L	
L			X	L	X	L	X	L				L	
	H			X		X		X					H
	X			H		X		X					H
	X			X		H		X					H
	X			X		X		H					H
	L			L		L		L					L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5		V	I _{OH} = MAX V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7			
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	0.35	0.5		
I _{IH}	C _N G ₀ , G ₂ G ₃ , P ₀ , P ₁ P ₂ P ₃ G ₁			20 140 80 60 40 160	μA	V _{IN} = 2.7 V V _{CC} = MAX
				0.1 0.7 0.4 0.3 0.2 0.8		
I _{IL}	C _N G ₀ , G ₂ G ₃ , P ₀ , P ₁ P ₂ P ₃ G ₁			-0.4 -2.8 -1.6 -1.2 -0.8 -3.2	mA	V _{IN} = 0.4 V V _{CC} = MAX
I _{OS}	Output Short-Circuit Current	-20		-100	mA	V _{CC} = MAX V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			12	mA	V _{CC} = MAX
				16		
	Total, Output LOW					

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AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	$(C_n \text{ to } C_{n+x}, C_{n+y}, C_{n+z})$		12 17	25 30	ns	$\bar{P}_0 = \bar{P}_1 = \bar{P}_2 = \bar{G}nd, \bar{G}_0 = \bar{G}_1 = \bar{G}_2 = 4.5\text{ V}$, Fig. 1
t_{PLH} t_{PHL}	$(\bar{P}_0, \bar{P}_1, \text{ or } \bar{P}_2 \text{ to } C_{n+x}, C_{n+y}, C_{n+z})$		9.0 10	21 22	ns	$\bar{P}_x = Gnd$ (if not under test), $C_n = \bar{G}_0 = \bar{G}_1 = \bar{G}_2 = 4.5\text{ V}$, Fig. 2
t_{PLH} t_{PHL}	$(\bar{G}_0, \bar{G}_1, \text{ or } \bar{G}_2 \text{ to } C_{n+x}, C_{n+y}, C_{n+z})$		9.0 10	21 22	ns	$\bar{G}_x = 4.5\text{ V}$ (if not under test), $C_n = \bar{P}_0 = \bar{P}_1 = \bar{P}_2 = Gnd$, Fig. 2
t_{PLH} t_{PHL}	$(\bar{P}_1, \bar{P}_2 \text{ or } \bar{P}_3 \text{ to } \bar{G})$		12 8.0	24 20	ns	$\bar{P}_x = Gnd$ (if not under test), $\bar{G}_0 = \bar{G}_1 = \bar{G}_2 = \bar{G}_3 = C_n = 0.0\text{ V}$, Fig. 1
t_{PLH} t_{PHL}	$(\bar{G}_0, \bar{G}_1, \bar{G}_2 \text{ or } \bar{G}_3 \text{ to } \bar{G})$		13 8.0	25 20	ns	$\bar{G}_x = 4.5\text{ V}$ (if not under test), $\bar{P}_1 = \bar{P}_2 = \bar{P}_3 = Gnd$, Fig. 1
t_{PLH} t_{PHL}	$(\bar{P}_0, \bar{P}_1, \bar{P}_2 \text{ or } \bar{P}_3 \text{ to } \bar{P})$		12 8.0	24 20	ns	$\bar{P}_x = Gnd$ (if not under test), Fig. 1

AC WAVEFORMS

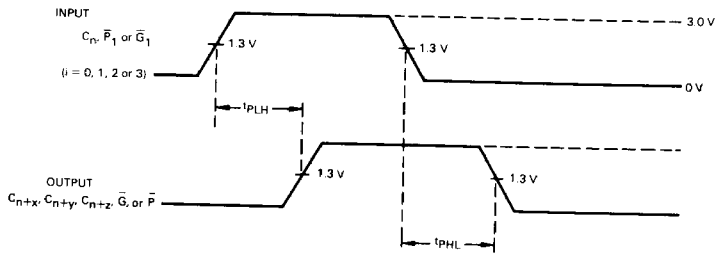


Fig. 1

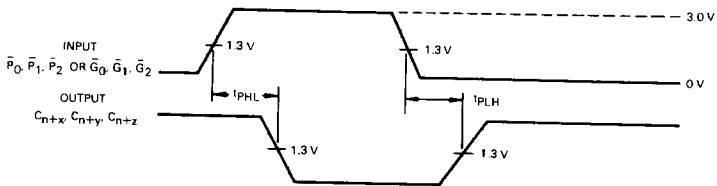


Fig. 2