

SN5407, SN5417, SN7407, SN7417 HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

SDLS032G – DECEMBER 1983 – REVISED MAY 2004

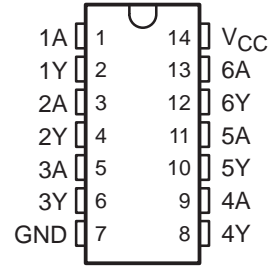
- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits

description/ordering information

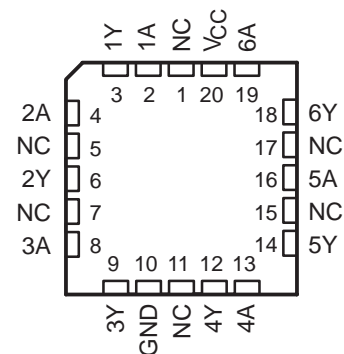
These TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS) or for driving high-current loads (such as lamps or relays) and also are characterized for use as buffers for driving TTL inputs. The SN5407 and SN7407 have minimum breakdown voltages of 30 V, and the SN5417 and SN7417 have minimum breakdown voltages of 15 V. The maximum sink current is 30 mA for the SN5407 and SN5417 and 40 mA for the SN7407 and SN7417.

These devices perform the Boolean function $Y = A$ in positive logic.

SN5407, SN5417 . . . J OR W PACKAGE
SN7407, SN7417 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN5407 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T _A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	SOIC – D	Tube	SN7407D	
		Tape and reel	SN7407DR	
	PDIP – N	Tube	SN7417D	
		Tape and reel	SN7417DR	
	SOP – NS	Tape and reel	SN7407NSR	SN7407
			SN7417NSR	SN7417
–55°C to 125°C	CDIP – J	Tube	SNJ5407J	
	CFP – W	Tube	SNJ5417J	
	LCCC – FK	Tube	SNJ5407W	SNJ5407W
		Tube	SNJ5407FK	SNJ5407FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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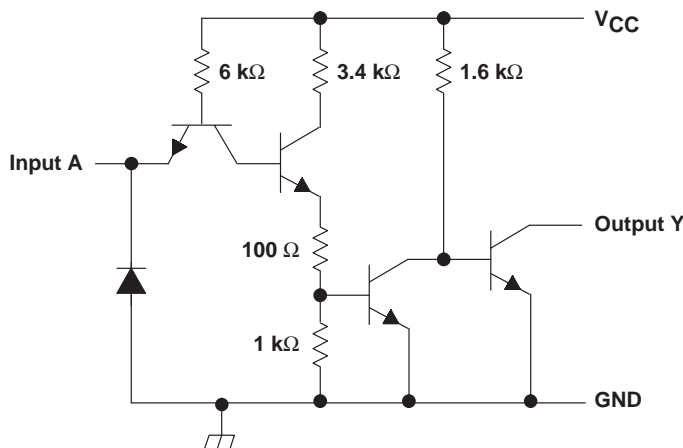
description/ordering information (continued)

These circuits are completely compatible with most TTL families. Inputs are diode clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 145 mW, and average propagation delay time is 14 ns.

logic diagram, each buffer/driver (positive logic)



schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I (see Note 1)	5.5 V
Output voltage, V_O (see Notes 1 and 2): SN5407, SN7407	30 V
SN5417, SN7417	15 V
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.
 2. This is the maximum voltage that should be applied to any output when it is in the off state.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT		
V _{CC}	Supply voltage	SN5407, SN5417	4.5	5	5.5	V	
		SN7407, SN7417	4.75	5	5.25		
V _{IH}	High-level input voltage	2			V		
V _{IL}	Low-level input voltage				0.8	V	
V _{OH}	High-level output voltage	SN5407, SN7407			30	V	
		SN5417, SN7417			15		
I _{OL}	Low-level output current	SN5407, SN5417			30	mA	
		SN7407, SN7417			40		
T _A	Operating free-air temperature	SN5407, SN5417	-55			125	°C
		SN7407, SN7417	0			70	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT	
V _{IK}	V _{CC} = MIN,	I _I = -12 mA			-1.5	V	
I _{OH}	V _{CC} = MIN,	V _{IH} = 2 V	V _{OH} = 30 V (SN5407, SN7407)		0.25	mA	
			V _{OH} = 15 V (SN5417, SN7417)		0.25		
V _{OL}	V _{CC} = MIN,	V _{IL} = 0.8 V	I _{OL} = 16 mA		0.4	V	
			I _{OL} = 30 mA (SN5407, SN5417)		0.7		
			I _{OL} = 40 mA (SN7407, SN7417)		0.7		
I _I	V _{CC} = MAX,	V _I = 5.5 V			1	mA	
I _{IH}	V _{CC} = MAX,	V _{IH} = 2.4 V			40	μA	
I _{IL}	V _{CC} = MAX,	V _{IL} = 0.4 V			-1.6	mA	
I _{CCH}	V _{CC} = MAX				29	41	mA
I _{CCL}	V _{CC} = MAX				21	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

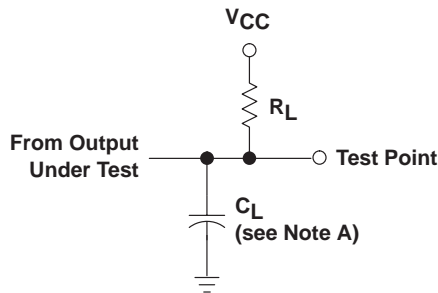
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A	Y	R _L = 110 Ω, C _L = 15 pF	6	10	ns	
t _{PHL}				20	30		
t _{PLH}	A	Y	R _L = 150 Ω, C _L = 50 pF	15		ns	
t _{PHL}				26			



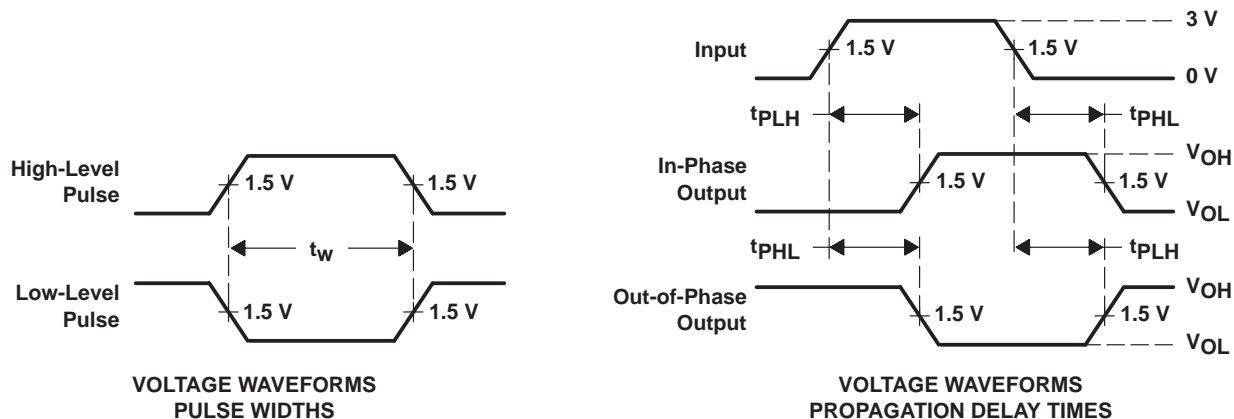
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 7$ ns, $t_f \leq 7$ ns.
 D. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
JM38510/00803BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/00803BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SN5407J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN5417J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN7407D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN7407DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN7407J	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
SN7407N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN7407N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN7407NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN7417D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN7417DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN7417N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN7417N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN7417NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ5407FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ5407J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ5407W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SNJ5417J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265