M74LS113AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET

DESCRIPTION

The M74LS113AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input $\overline{T}$, inputs J and K and direct set input $\overline{S_D}$.

FEATURES

- Negative edge-triggering
- Each flip-flop can be used independently
- Direct set input
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

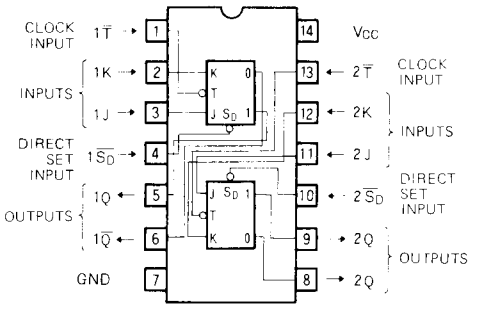
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While $\overline{T}$ is high, signals J and K are put in the read-in state, and when $\overline{T}$ changes from high to low, the J and K signals immediately before the change emerge in outputs Q and $\overline{Q}$ in accordance with the function table. By setting $\overline{S_D}$ low, Q and $\overline{Q}$ are set low and high respectively irrespective of the status of the other input signals. For use as a J-K flip-flop, $\overline{S_D}$ must be kept high.

The only difference in functions from M74LS112AP is that this IC has no $\overline{RD}$ input.

PIN CONFIGURATION (TOP VIEW)



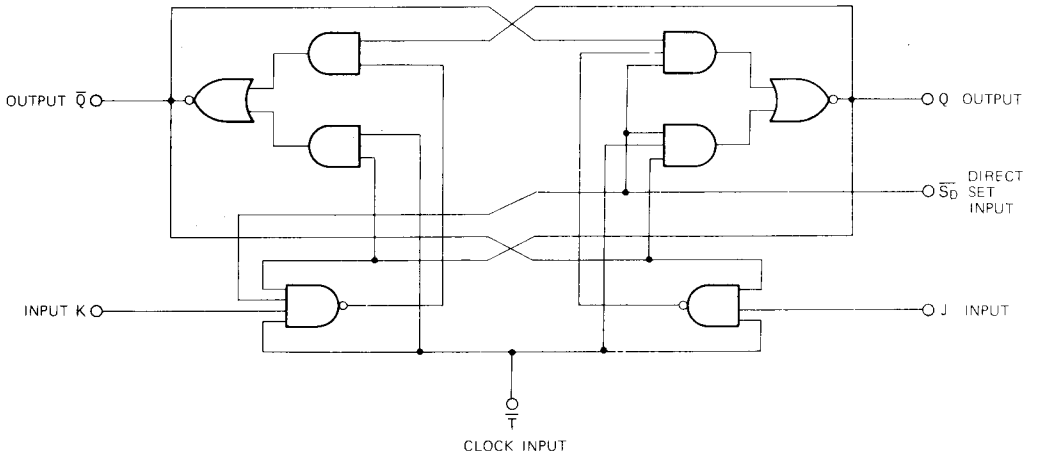
Outline 14P4

FUNCTION TABLE (Note 1)

T	$\overline{S_D}$	J	K	Q	$\overline{Q}$
X	L	X	X	H	L
↓	H	H	H	Toggle	
↓	H	L	H	L	H
↓	H	H	L	H	L
↓	H	L	L	Q^0	$\overline{Q}^0$
H	H	X	X	Q^0	$\overline{Q}^0$

Note 1 ↓ : Transition from high to low-level (negative edge trigger)
X : Irrelevant
Q^0 : level of Q before the indicated steady-state input conditions were established.
$\overline{Q}^0$: level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle : complement of previous state with ↓ transition of outputs.

BLOCK DIAGRAM (EACH FLIP-FLOP)



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ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	°C
T_{stg}	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	J, K	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{S_D}$					60	
		$\overline{T}$					80	
		J, K	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{S_D}$					0.3	
		$\overline{T}$					0.4	
I_{IL}	Low-level input current	J, K	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
		$\overline{S_D}$ $\overline{T}$					-0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			4	6	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: Supply current measurements should be done with Q and $\overline{Q}$ set alternately high and $\overline{T}$ should be set low during actual measurement.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 4)	30	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{T}$ to Q, $\overline{Q}$			8	20	ns
t_{PHL}				7	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{S_D}$ to Q, $\overline{Q}$			8	20	ns
t_{PHL}				7	20	ns

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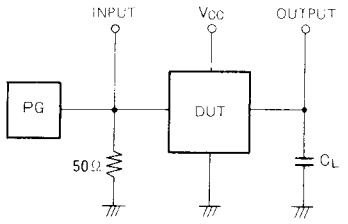
Note 4. Measurement circuit

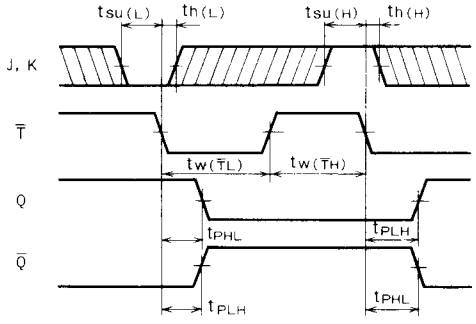


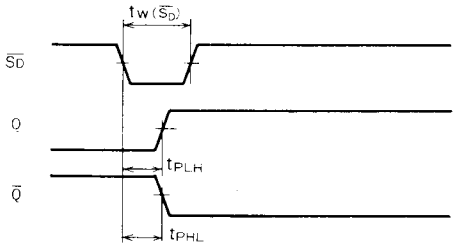
(1) The pulse generator (PG) has the following characteristics.
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{w(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	13		ns
$t_{w(\overline{S_D})}$	Direct set pulse width		25	10		ns
t_r	Clock rise time			650	100	ns
t_f	Clock fall time			900	100	ns
$t_{SU(H)}$	Setup time high J, K to $\overline{T}$		20	9		ns
$t_{SU(L)}$	Setup time low J, K to $\overline{T}$		20	12		ns
$t_{h(H)}$	Hold time high J, K to $\overline{T}$		0	−10		ns
$t_{h(L)}$	Hold time low J, K to $\overline{T}$		0	−5		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.

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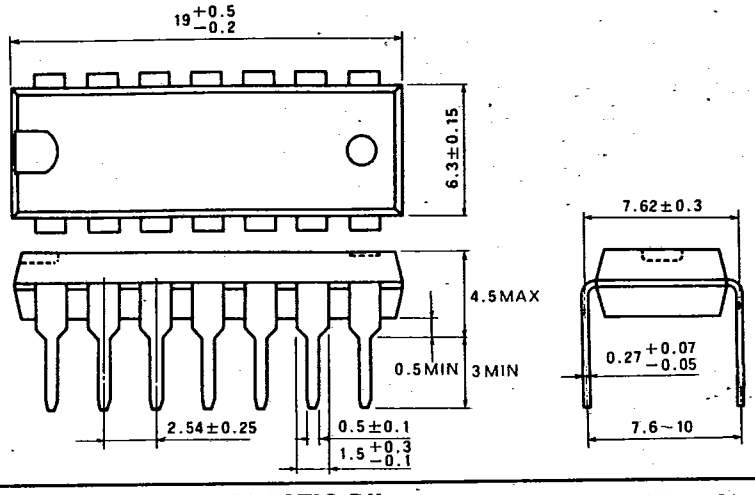
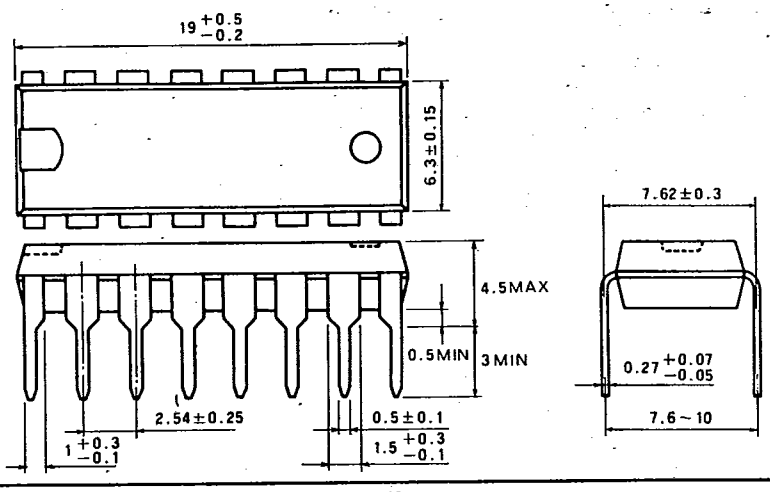
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm