M74LS109AP

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

DESCRIPTION

The M74LS109AP is a semiconductor integrated circuit containing 2 J-$\overline{K}$ positive edge-triggered flip-flop circuits with discrete terminals for clock input T, inputs J and $\overline{K}$, and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Positive edge-triggering
- Each flip-flop can be used independently
- Direct set and reset inputs
- J and $\overline{K}$ inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20~+75°C)

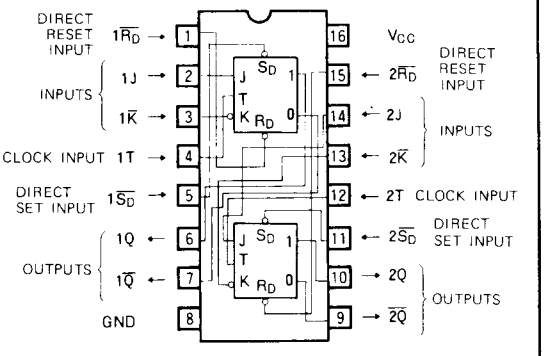
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

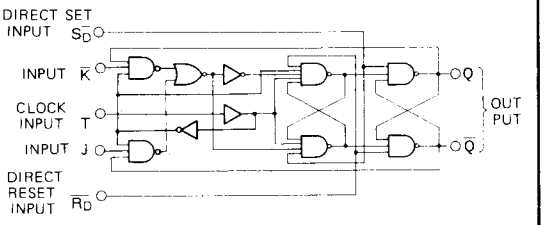
When T changes from low to high, the J and $\overline{K}$ signals immediately before the change emerge in outputs Q and $\overline{Q}$ in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into a direct R-S flip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, Q = $\overline{Q}$ = high. However, when both of them change to high at the same time, the status of Q and $\overline{Q}$ cannot be anticipated. For use as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high. By connecting J and $\overline{K}$, this IC can be used as a D-type flip-flop.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM (EACH FLIP-FLOP)



FUNCTION TABLE (Note 1)

$\overline{S_D}$	$\overline{R_D}$	T	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	L	X	X	Q^0	$\overline{Q^0}$
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q^0	$\overline{Q^0}$
H	H	↑	H	H	H	L

Note 1 ↑ : Transition from low to high-level (positive edge trigger)
Q^0 : Level of Q before the indicated steady-state input conditions were established.
$\overline{Q^0}$: Level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle : complement of previous state with ↑ transition of output
X : Irrelevant
* : Q = $\overline{Q}$ = high when $\overline{S_D}$ = $\overline{R_D}$ = low and so when both $\overline{S_D}$ and $\overline{R_D}$ are set high, the status of Q and $\overline{Q}$ cannot be anticipated.

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +5.5	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ + 75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ + 75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_I = 0.8V V_I = 2 V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 4 mA		0.25	0.4	V
			V_I = 0.8V, V_I = 2 V	I_{OL} = 8 mA		0.35	0.5	V
I_{IH}	High-level input current	J, $\overline{K}$, T	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		$\overline{S_D}$, $\overline{R_D}$					40	
		J, $\overline{K}$, T	V_{CC} = 5.25V, V_I = 10V				0.1	mA
		$\overline{S_D}$, $\overline{R_D}$					0.2	
I_{IL}	Low-level input current	J, $\overline{K}$, T	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
		$\overline{S_D}$, $\overline{R_D}$					−0.8	
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0 V		−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25V, (Note 3)			4	8	mA

* : All typical values are at V_{CC} = 5 V, T_a = 25℃

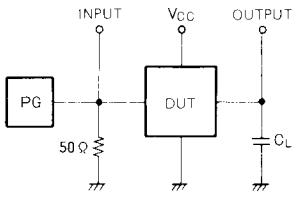
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: The supply current should be measured with Q and $\overline{Q}$ alternately set high and with T set low during actual measurement.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L = 15pF (Note 4)	25	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from T to Q, $\overline{Q}$			10	25	ns
t_{PHL}				12	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{S_D}$, $\overline{R_D}$ to Q, $\overline{Q}$			11	25	ns
t_{PHL}				10	40	ns

Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.

(2) C_L includes probe and jig capacitance.

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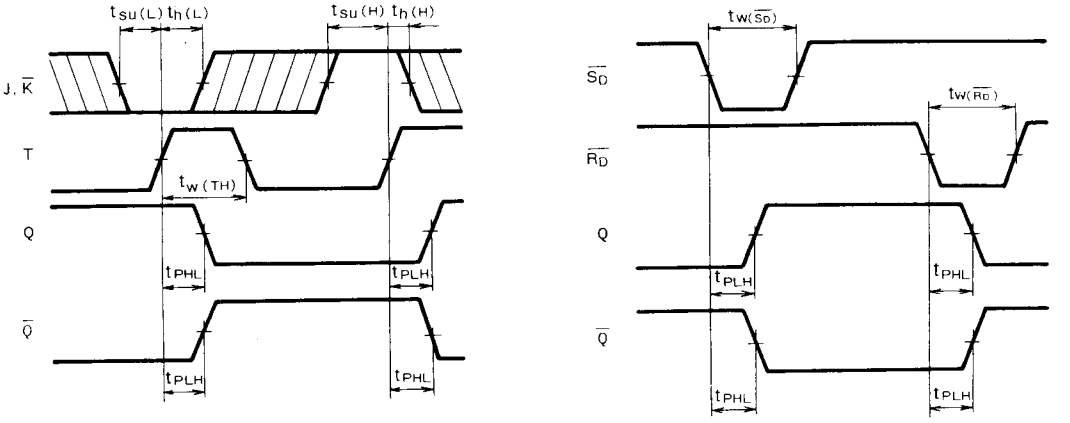
TIMING REQUIREMENTS (V_{CC} = 5 V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(TH)}$	Clock input T high pulse width		25	11		ns
$t_{w(\overline{SD}, \overline{RD})}$	Direct set, reset pulse width		25	4		ns
$t_{su(H)}$	Setup time high to T		20	19		ns
$t_{su(L)}$	Setup time low to T		20	7		ns
$t_{h(H)}$	Hold time high to T		5	−2		ns
$t_{h(L)}$	Hold time low to T		5	−16		ns

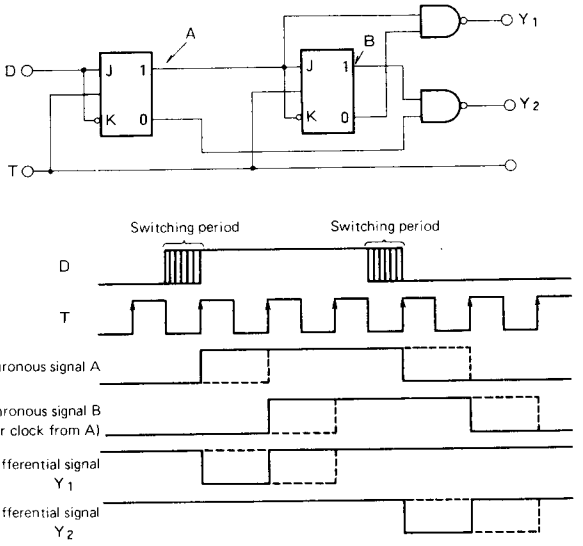
TIMING DIAGRAM (Reference level = 1.3V)



Note 4: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

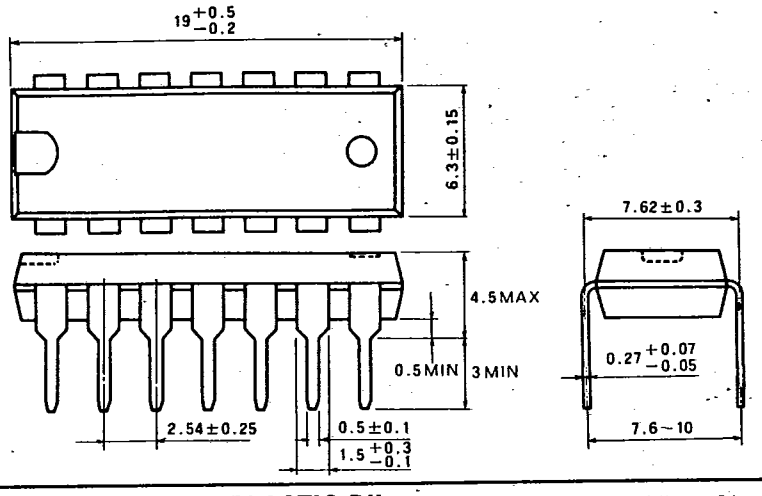
Typical circuit for converting asynchronous signal into synchronous signal and rise/fall differential circuit



Note 5: The waveforms indicated by the dotted lines apply when reading with the next clock without observing the set-up time to T.

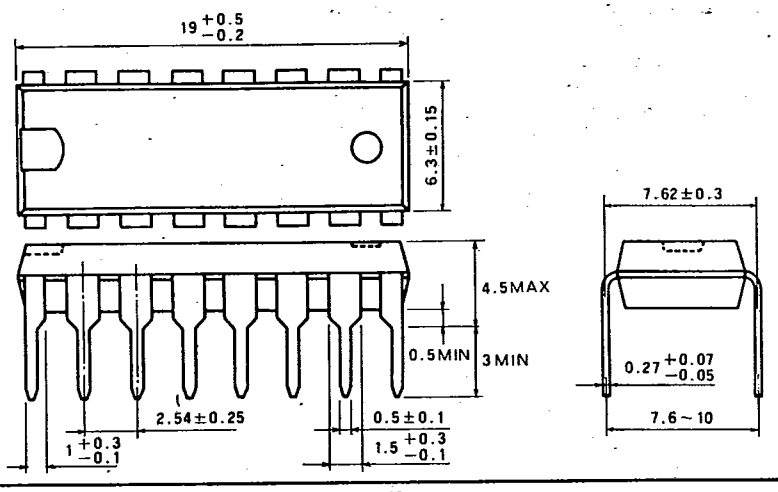
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm