

MITSUBISHI LSI's M58658P

320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58658P is a serial input/output 320 bit electrically erasable and reprogrammable ROM organized as 20 words of 16 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage 10 years (min)
- Write/erase time 20ms word
- Typical power supply voltages -30V, +5V
- Number of erase-write cycles 10^5 times (min)
- Number of read access unrefreshed. . . 10^9 times (min)
- 5V I/O interface

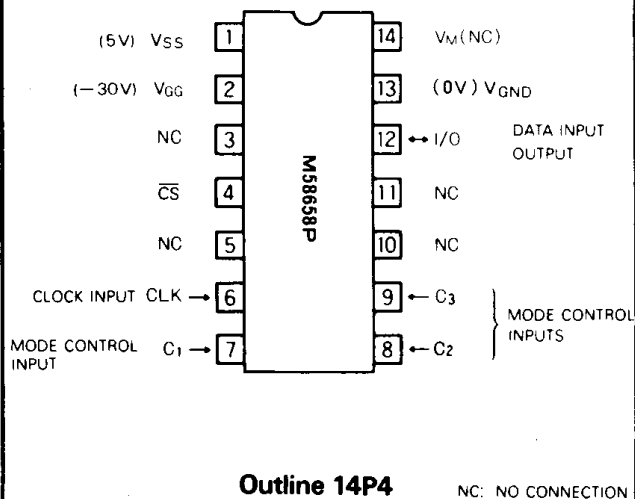
APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

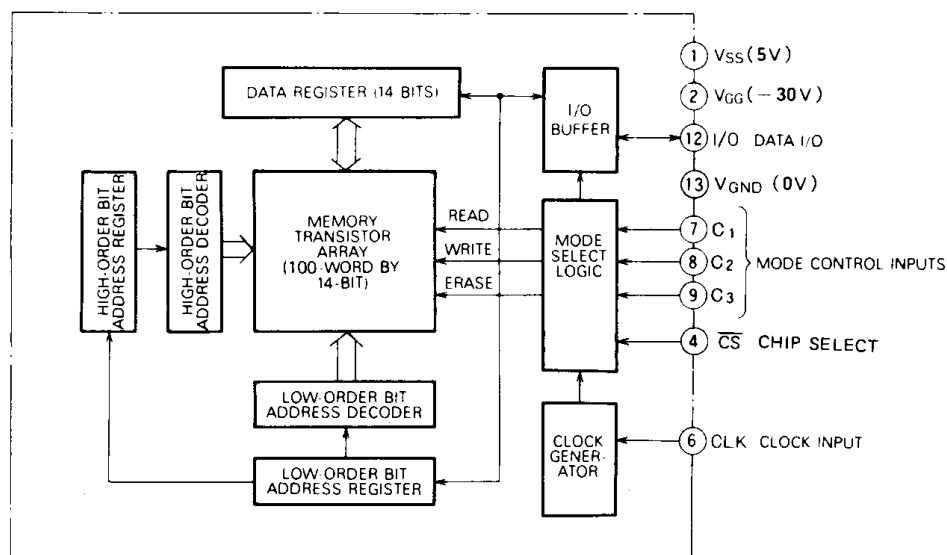
FUNCTION

The address is designated by two consecutive one-of-four coded digits. Eight modes—accept address, AD accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1 , C_2 , and C_3 . Data is stored by internal negative writing pulses that selectively tunnel charges into the $\text{SiO}_2\text{--Si}_3\text{N}_4$ interface of the gate insulators of the MNOS memory transistors.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address AD accept address and accept data modes, used for input. In the shift data output mode, used for output. In the standby, read, erase and write modes, this pin is in a floating state
V _M	Test	Used for testing purposes only. It should be left unconnected during normal operation.
V _{SS}	Chip substrate voltage	Normally connected to +5V.
V _{GG}	Power supply voltage	Normally connected to -30V.
CLK	Clock input	Required for all operating modes, when $\overline{CS}$ is low.
C ₁ ~ C ₃	Mode control input	Used to select the operation mode
V _{GND}	Ground voltage	Connected to ground (0V)
$\overline{CS}$	Chip select	Used for chip selection in "L"

OPERATION MODES

C ₁	C ₂	C ₃	Functions
H	H	H	Standby mode: The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state.
H	H	L	Additional data (AD) accept address: Data presented at the I/O pin is shifted into the AD address registers one bit with each clock pulse. The address is designated by two one-of-four coded digits. 4-word address is assigned in this mode.
H	L	H	Erase mode: The word stored at the addressed location is erased. The data bits after erasing are all low-level.
H	L	L	Accept address mode: Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-four-coded digits. 16-word address is assigned in this mode.
L	H	H	Read mode: The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode: The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode: The data contained in the data register is written into the location designated by the address registers.
L	L	L	Accept data mode: The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{GG}	Supply voltage	With respect to V _{SS}	0.3 ~ -40	V
V _I	Input voltage		0.3 ~ -20	V
V _O	Output voltage		0.3 ~ -20	V
T _{stg}	Storage temperature		-40 ~ 125	°C
T _{opr}	Operating temperature		-10 ~ 70	°C

RECOMMENDED OPERATING CONDITIONS (T_a = -10 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{GG} -V _{SS}	Supply voltage	-32.2	-35	-37.8	V
V _{SS} -V _{GND}	Supply voltage	4.75	5	6	V
V _{IH}	High-level input voltage	V _{SS} - 1		V _{SS} + 0.3	V
V _{IL}	Low-level input voltage	V _{SS} - 6.5		V _{SS} - 4.25	V

320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

ELECTRICAL CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{GG}-V_{SS} = -35\text{V} \pm 8\%$, $V_{SS}-V_{GND} = 5\text{V} \pm 5\%$, $+20\%$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		$V_{SS} - 1$		$V_{SS} + 0.3$	V
V_{IL}	Low-level input voltage		$V_{SS} - 6.5$		$V_{SS} - 4.25$	V
I_{IL}	Low-level input current CLK, C1, C2, C3, I/O	$V_I - V_{SS} = -6.5\text{V}$	-10		+10	μA
R_I	Input pull-up resistance, $\overline{CS}$			30		k Ω
I_{OZL}	Off-state output current, low-level voltage applied	$V_O - V_{SS} = -6.5\text{V}$	-10		+10	μA
V_{OH}	High-level output voltage	$I_{OH} = -200\mu\text{A}$	$V_{SS} - 1$			V
V_{OL}	Low-level output voltage	$I_{OL} = 10\mu\text{A}$			$V_{GND} + 0.5$	V
I_{GG}	Supply current from V_{GG}	$I_O = 0\mu\text{A}$		5.5	8.8	mA

Note 1: Typical values are at $T_a = 25^\circ\text{C}$ and $V_{GG}-V_{SS} = -35\text{V}$.

TIMING REQUIREMENTS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{GG}-V_{SS} = -35\text{V} \pm 8\%$, $V_{SS}-V_{GND} = 5\text{V} \pm 5\%$, $+20\%$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$T_{L(\phi)}$	Negative clock pulse width		30			μs
$T_{H(\phi)}$	Positive clock pulse width		33			μs
$T(\phi)$	Clock period				300	μs
t_w	Write time		16	20	24	ms
t_E	Erase time		16	20	24	ms
t_r, t_f	Risetime, fall time				1	μs
t_{su}	Control setup time before the fall of the clock pulse		1			μs
t_h	Control hold time after the rise of the clock pulse		0			μs
t_{ss}	Clock control setup time before the fall of $\overline{CS}$		1			μs
t_{hs}	Clock control hold time after the rise of $\overline{CS}$		1			μs

SWITCHING CHARACTERISTICS ($T_a = -10 \sim 70^\circ\text{C}$, $V_{GG} = -35\text{V} \pm 8\%$, unless otherwise noted)

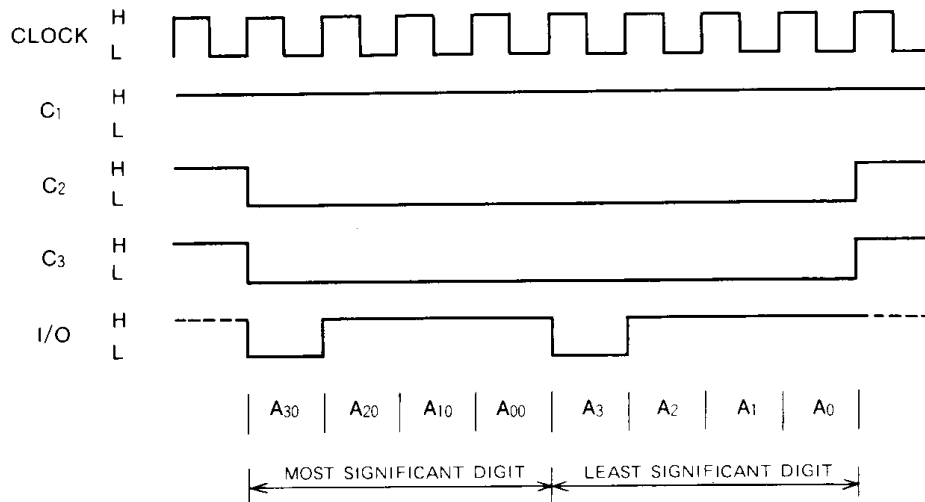
Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(c)}$	Read access time	t_{PW}	$C_L = 100\text{pF}$, $V_{OH} = V_{SS} - 2\text{V}$, $V_{OL} = V_{GND} + 1.5\text{V}$			20	μs
t_s	Unpowered nonvolatile data retention time	T_S	$N_{EW} = 10^4$, $t_w(W) = 20\text{ms}$, $t_w(E) = 20\text{ms}$	10			Year
		T_S	$N_{EW} = 10^5$, $t_w(W) = 20\text{ms}$, $t_w(E) = 20\text{ms}$	1			
N_{EW}	Number of erase/write cycles	N_W		10^5			Times
N_{RA}	Number of read access unrefreshed	N_{RA}		10^9			Times
t_{dv}	Data valid time	t_{PW}				20	μs

320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

TIMING DIAGRAM

Accept Address Mode (8 clocks)

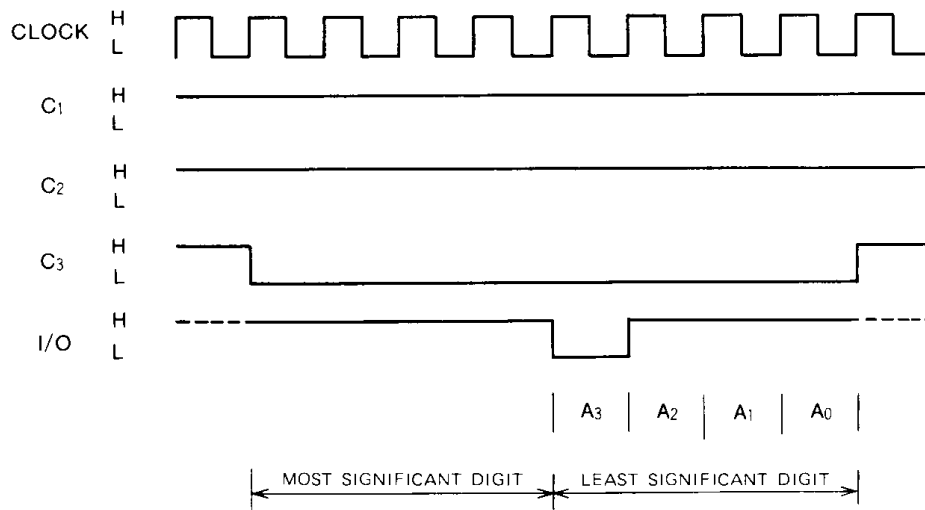
$\overline{CS} : L$



Note 2: The addresses from A_{00} to A_{33} are designated by two one-of-four coded digits. The above figure shows designation of address A_{33} (decimal address 15).

AD Accept Address Mode (8 clocks)

$\overline{CS} : L$

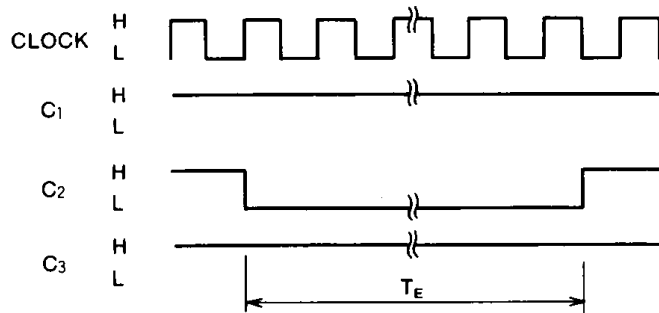


Note 3: In the AD accept address mode, the higher four are set high, and the lower four digits are designated by one of the four coded digits. This address mode allows designation of addresses from A_0 to A_3 . Each address has a 16 bits. The above figure shows designation of address A_3 .

320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

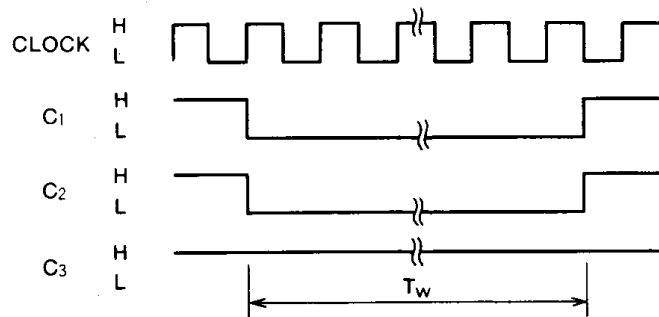
Erase Mode

$\overline{CS} : L$



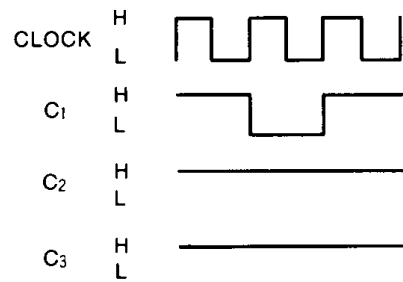
Write Mode

$\overline{CS} : L$



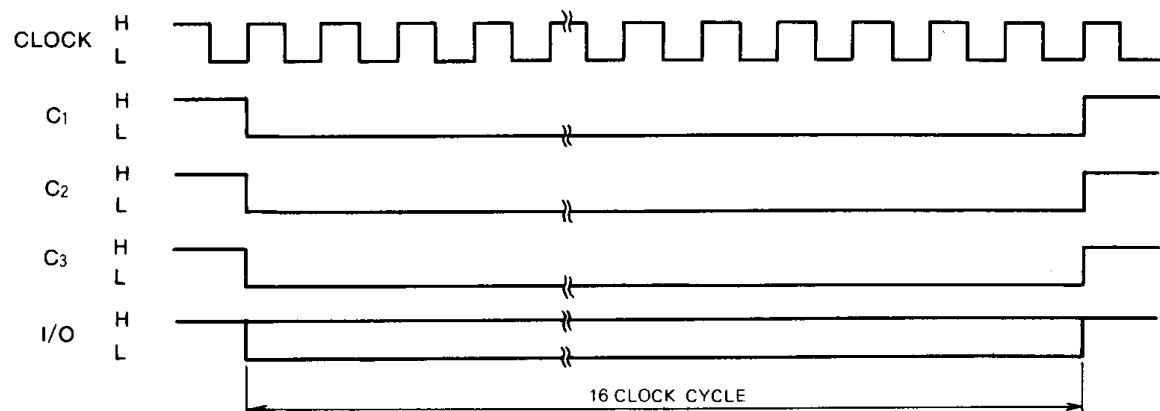
Read Mode (1 clock)

$\overline{CS} : L$



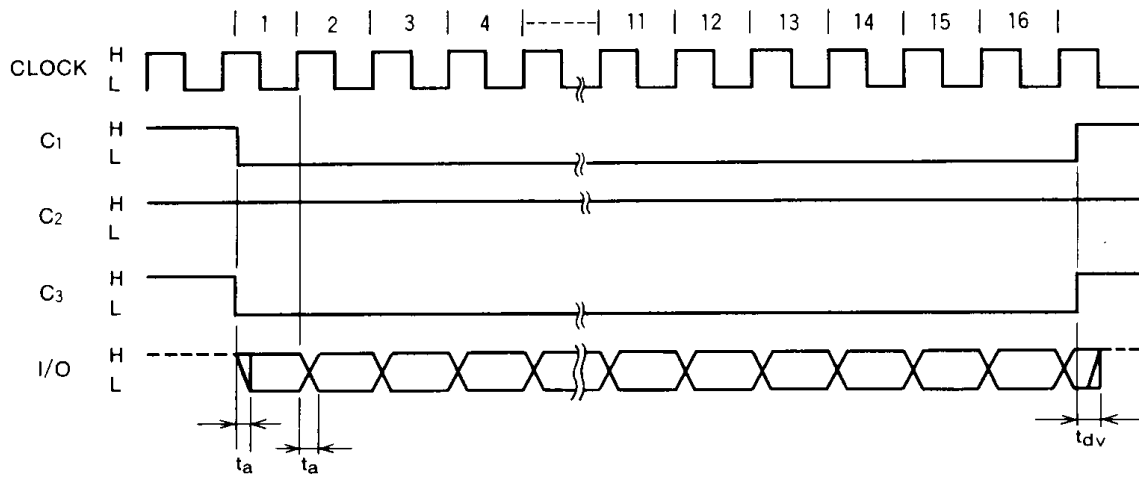
Accept Data (16 clocks)

$\overline{CS} : L$

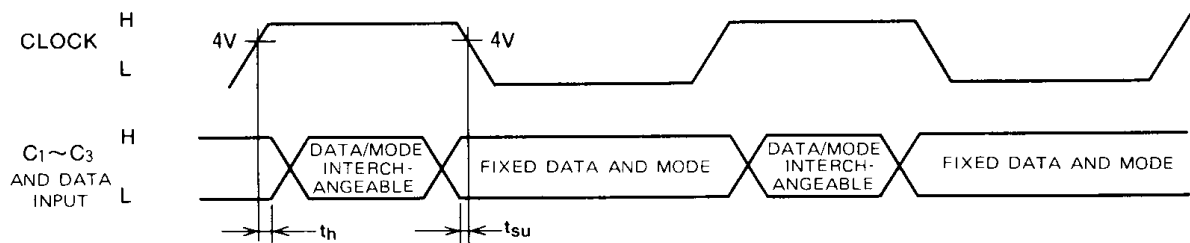


320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

Shift Data Output Mode (16 clocks) $\overline{CS} : L$

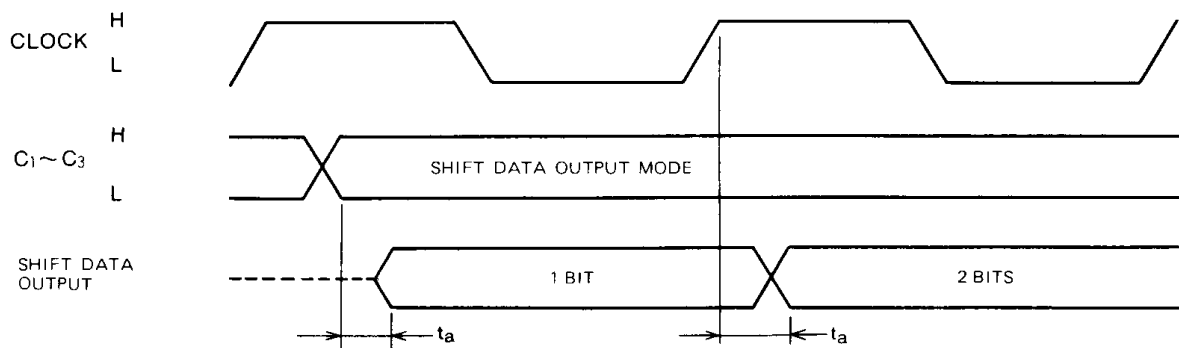


Timing of clock, C_1 , C_2 , C_3 , and data input



Note 4: $C_1 \sim C_3$ and accept data (AD accept data) are interchangeable while the clock is set high.

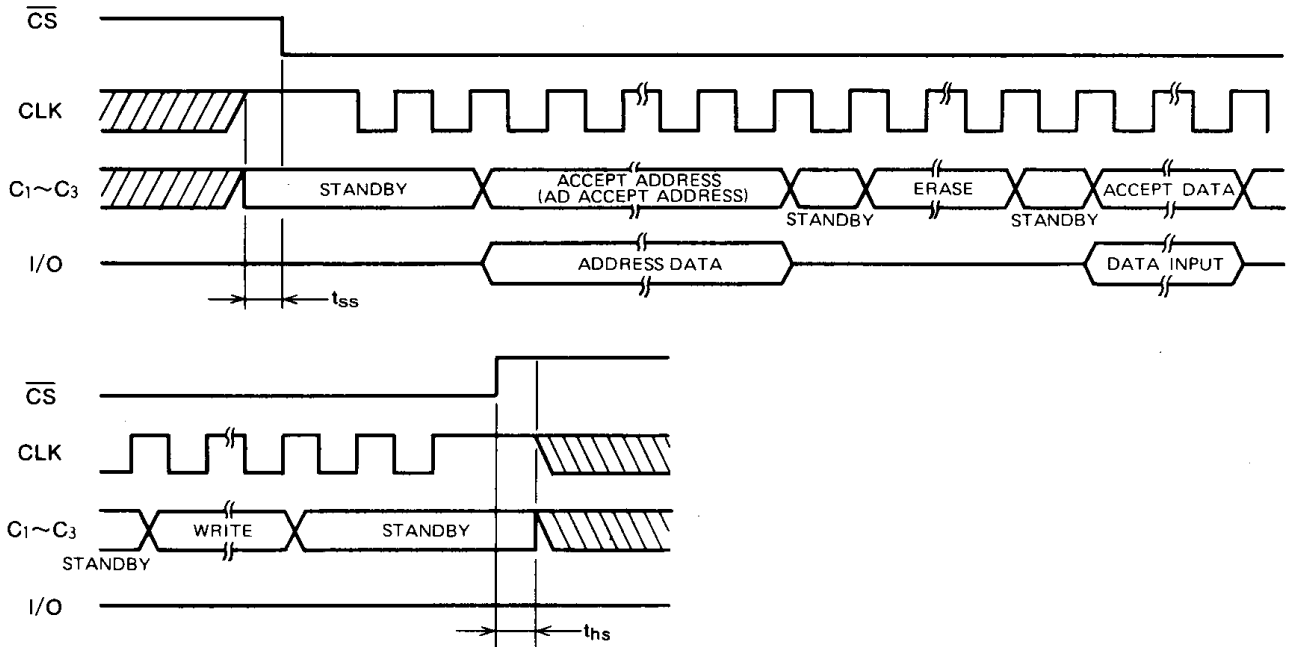
Timing of clock, C_1 , C_2 , C_3 , and data input



320-BIT (20-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

Operation flowchart

Rewriting flowchart

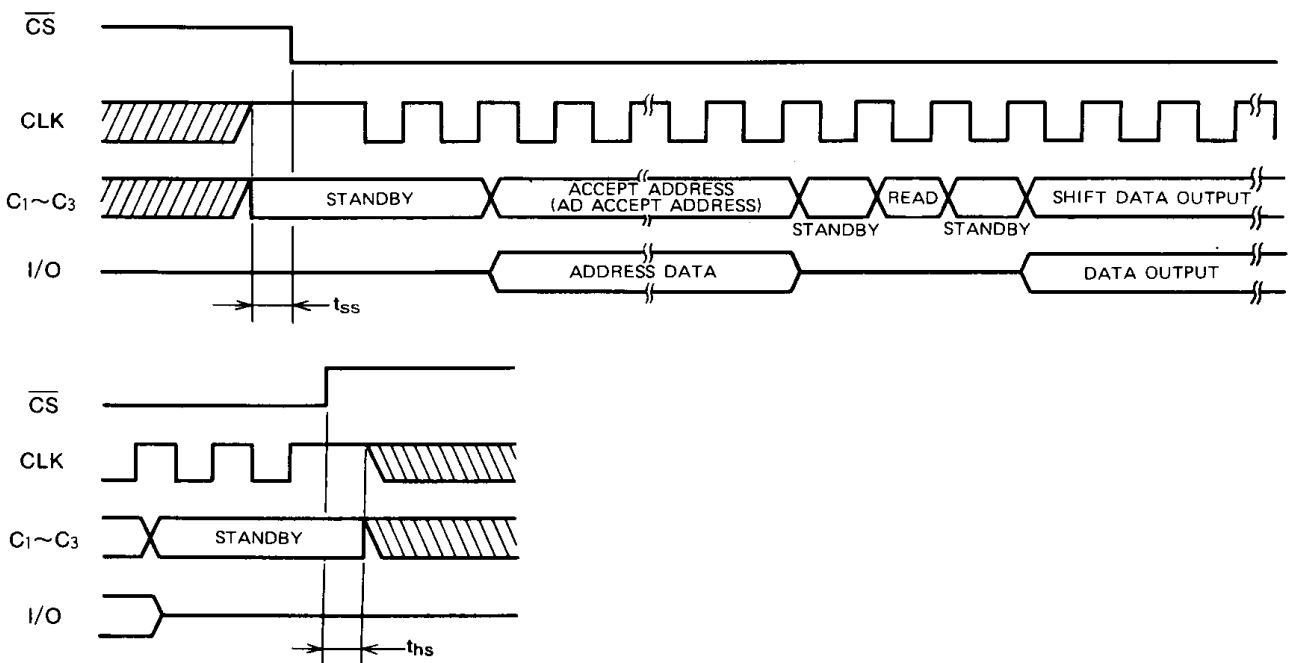


Note 5: One or more clock are required for standby between modes.

6: Set $\overline{CS}$ to the low level after the lapse of t_{ss} and CLK has been set high and $C_1 \sim C_3$ have been set to the standby mode.

7: Keep CLK to the high level and $C_1 \sim C_3$ to "standby" from the time when $\overline{CS}$ is set high to the lapse of t_{hs} .

Read Flowchart



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Power-on/off Conditions

With power-on, V_{GG} is applied after V_{SS} has been applied.
 With power-off, V_{SS} is cut after V_{GG} has been cut. For power-on and off, hold $\overline{CS}$ in V_{SS} or floating state. The recommended timing chart for power-on and off is as follows.

