

SANYO

No.1086C

LA7820

Monolithic Linear IC

Color TV Synchronization, Deflection Circuit

The LA7820 is an IC containing not only the main functions required to achieve synchronization and deflection in color television receivers but also a generator of horizontal, vertical blanking pulses and a generator of burst gate pulses (sand castle type). It is a multifunctional IC ideally suited for use in color television receivers aiming at high-quality picture reproduction.

Functions

- Synchronizing separation
- Horizontal AFC
- Composite castle pulse (burst gate pulse + horizontal blanking pulse)
- Composite blanking pulse (vertical + horizontal blanking pulse)
- Vertical oscillation
- Horizontal oscillation
- Vertical drive
- X-ray protection

Features

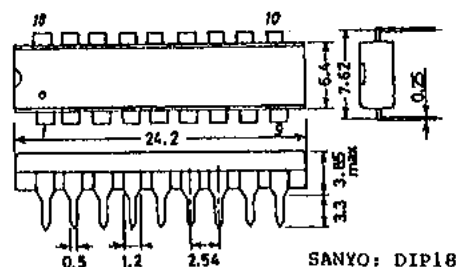
- Horizontal and vertical oscillations are stable against variations in ambient temperature and supply voltage due to small warm-up drift.
- Small variation in horizontal oscillation frequency
- Good linearity and interlace because DC bias at vertical output stage is subjected to sampling control within retrace time.
- Vertical blanking pulse width can be set freely by peripheral parts.
- Minimized picture distortion because AFC circuit is defeated during vertical trigger pulse input period.
- Multifunctional and compact (DIP-18).

Maximum Ratings at $T_a = 25^\circ\text{C}$

Maximum Supply Voltage	V_{CC14}	14	V
Maximum Supply Current	I_{CC18}	16	mA
Maximum Applied Voltage	V_{11}	-6	V
Allowable Power Dissipation	$P_{d\max}$ $T_a = 60^\circ\text{C}$	570	mW
Operating Temperature	T_{opg}	-20 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

Recommended Supply Voltage	V_{CC14}	12	V
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Case Outline 3007A-D18IC
 (unit: mm)


The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass-produced. The information herein is believed to be accurate and reliable. However, no responsibility is assumed by SANYO for its use, nor for any infringements of patents or other rights of third parties which may result from its use.

Specifications and information herein are subject to change without notice.

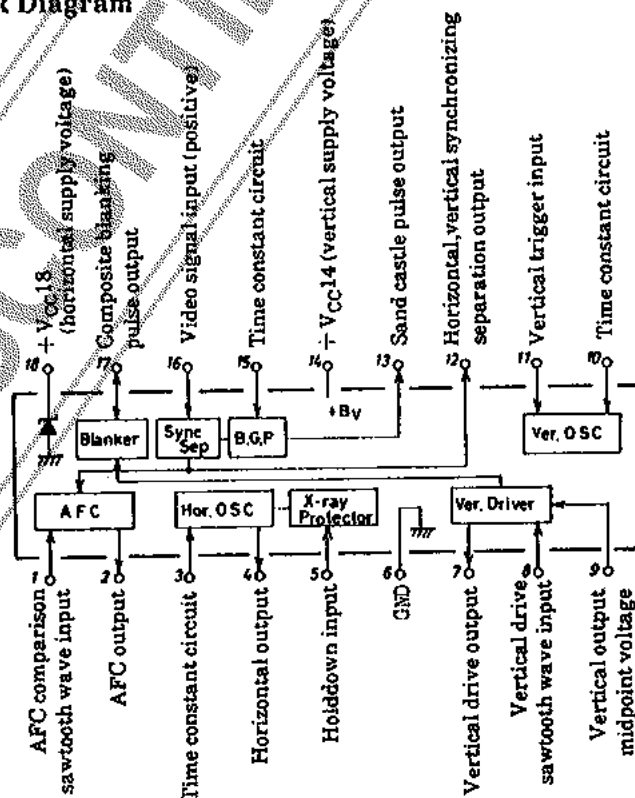
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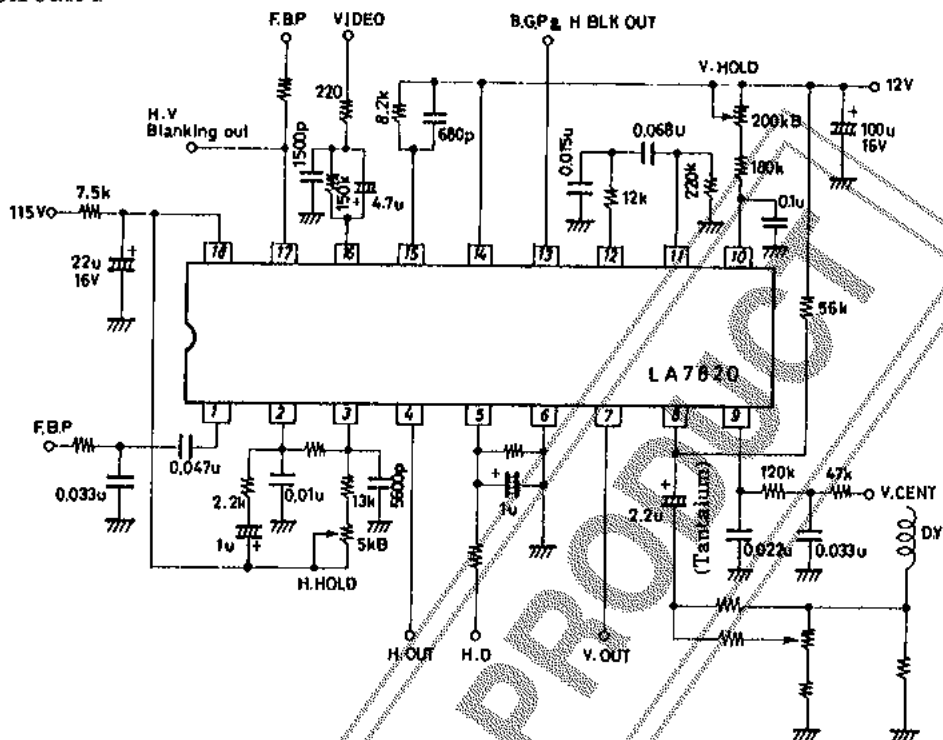
Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC14} = 12\text{V}$, See Test Circuit.

		min	typ	max	unit
V_{CC14} Current Dissipation	I_{CC14}	13.5		29.0	mA
V_{CC18} Supply Voltage	V_{CC18}	11.8		13.2	V
Zener Bias Minimum Current				13	mA
Sync Separation Input DC Level		9.0		9.6	V
Sync Signal Peak Value		9.5		11.5	V
Burst Gate Pulse Peak Value (SCP)		9.5		11.5	V
Burst Gate Pulse Leading Edge Delay Time 1 (SCP)	T_{BR}			0.5	μs
Burst Gate Pulse Leading Edge Delay Time 2 (SCP)	T_{BR}	3.6		4.2	μs
Horizontal Blanking Pulse Peak Value (SCP)		2.7		3.3	V
Horizontal Blanking Pulse Peak Value (CBP)	$I = 1\text{mA}$	12.7		13.5	V
Vertical Blanking Pulse Peak Value (CBP)	Load resistance $R = 33\text{k}\Omega$	7.2		8.2	V
Vertical Frequency Pull-in Range	Vertical sync 60Hz	9.0		11.0	Hz
Vertical Free-running Frequency	f_v $V_{R1} = f_v$ center 55Hz	50		60	Hz
Supply Voltage Dependence of Vertical Frequency	$V_{14} = 12 \pm 1\text{V}$, 55Hz at 12V	-0.5		0.5	Hz
Midpoint Control Threshold Level		3.8		4.4	V
Vertical Blanking Threshold Level		5.0		5.7	V
Vertical Oscillation Start Voltage				4	V
Temperature Characteristic of Vertical Frequency	$T_a = -10$ to $+60^\circ\text{C}$	-0.028		0.028	Hz/ $^\circ\text{C}$
Vertical Driver Amplification Factor		12		17	dB
Horizontal AFCDC Loop Gain	+ sign at $V_1 = 5\text{V}$, - sign at $V_1 = 1\text{V}$	± 0.6		± 1.5	mA
Horizontal Free-running Frequency	f_H f_H center 15.734kHz	-750		750	Hz
Horizontal Oscillation Start Voltage				4	V
Supply Voltage Dependence of Horizontal Frequency	$V_Z - V_Z \times 99\%$	-50		50	Hz

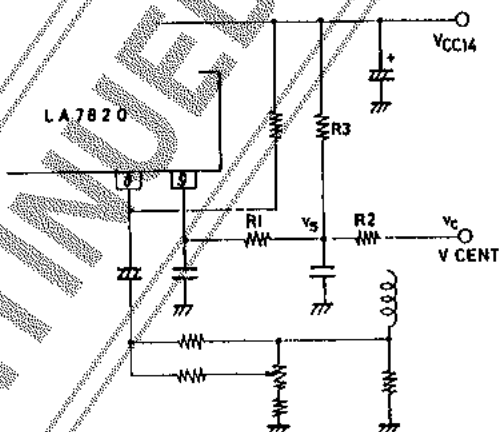
Equivalent Circuit Block Diagram



Sample Application Circuit 1



Sample Application Circuit 2



Application where the vertical output circuit is operated from Low B

If the vertical output circuit is operated from Low B (12V), the configuration is Sample Application Circuit 1. This may cause the output DC bias to be unstable. This occurs when the output midpoint voltage is made lower than the reference voltage ($0.433V_{CC}$) on pin 9 (DC feedback pin of IC). Sample Application Circuit 2 can be used to prevent this phenomenon. As shown above, V_{CC} and output midpoint voltage V_C are divided by R_2 , R_2 and feedback is applied to pin 9 from this divided voltage V_S ($V_S > V_C$). R_2 , R_3 must be set so that $0.433V_{CC} < V_S$ is yielded.