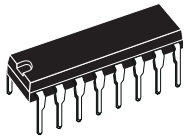
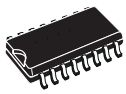
HCF4089B

BINARY RATE MULTIPLIER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO "15" INPUT AND "15" DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP



SOP

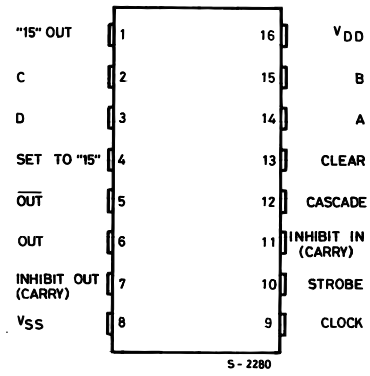
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4089BEY	
SOP	HCF4089BM1	HCF4089M013TR

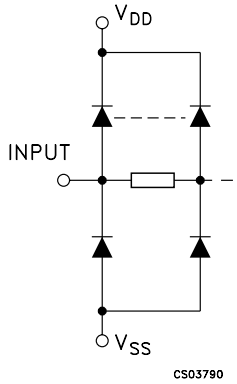
DESCRIPTION

HCF4089B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
HCF4089B is a low power 4-bit digital rate multiplier that provides an output pulse rate that is the clock input pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, ther will be 13 output pulses for every 16 input pulses.
HCF4089B has an internal synchronous 4-bit counter, which, together with one of the four binary inputs bits, produces pulse trains as shown in the timing diagram.
If more than one binary input bit is high, the resulting pulse train is a combination of the above separate pulse trains. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebrical and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversions, and frequency division.

PIN CONNECTION



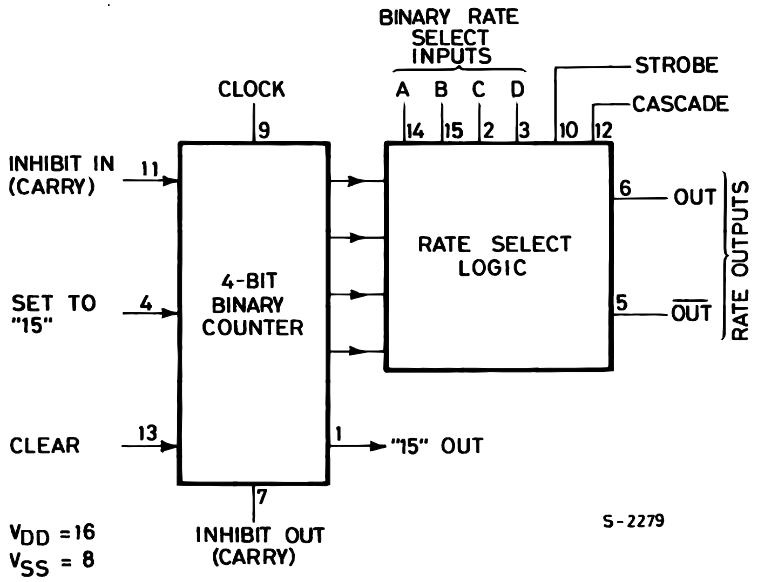
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
14, 15, 2, 3	A, B, C, D	Binary Rate Select Inputs
5	$\overline{OUT}$	Rate Output
6	OUT	Rate Output
4	SET TO "15"	Set Input
1	"15" OUT	Output
7	INHIBIT OUT (CARRY)	Inhibit Out (Carry)
13	CLEAR	Clear Input
12	CASCADE	Cascade
11	INHIBIT IN (CARRY)	Inhibit Input (Carry)
10	STROBE	Strobe
9	CLOCK	Clock Input
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



TRUTH TABLE

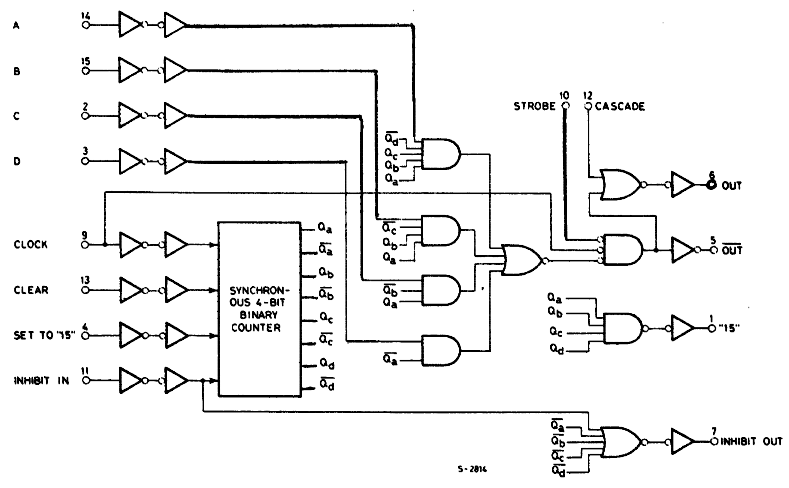
INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level										Number of Pulses or Output Logic Level			
D	C	B	A	CLOCK	INH IN	STR.	CAS.	CLEAR	SET	OUT	$\overline{OUT}$	INH OUT	"15" OUT
L	L	L	L	16	L	L	L	L	L	L	H	1	1
L	L	L	H	16	L	L	L	L	L	1	1	1	1
L	L	H	L	16	L	L	L	L	L	2	2	1	1
L	L	H	H	16	L	L	L	L	L	3	3	1	1
L	H	L	L	16	L	L	L	L	L	4	4	1	1
L	H	L	H	16	L	L	L	L	L	5	5	1	1
L	H	H	L	16	L	L	L	L	L	6	6	1	1
L	H	H	H	16	L	L	L	L	L	7	7	1	1
H	L	L	L	16	L	L	L	L	L	8	8	1	1
H	L	L	H	16	L	L	L	L	L	9	9	1	1
H	L	H	L	16	L	L	L	L	L	10	10	1	1
H	L	H	H	16	L	L	L	L	L	11	11	1	1
H	H	L	L	16	L	L	L	L	L	12	12	1	1
H	H	L	H	16	L	L	L	L	L	13	13	1	1
H	H	H	L	16	L	L	L	L	L	14	14	1	1
H	H	H	H	16	L	L	L	L	L	15	15	1	1
X	X	X	X	16	H	L	L	L	L	•	•	H	•
X	X	X	X	16	L	H	L	L	L	L	H	1	1
X	X	X	X	16	L	L	H	L	L	H	*	1	1
H	X	X	X	16	L	L	L	H	L	16	16	H	L
L	X	X	X	16	L	L	L	H	L	L	H	H	L
X	X	X	X	16	L	L	L	L	H	L	H	L	H

X : Don't Care

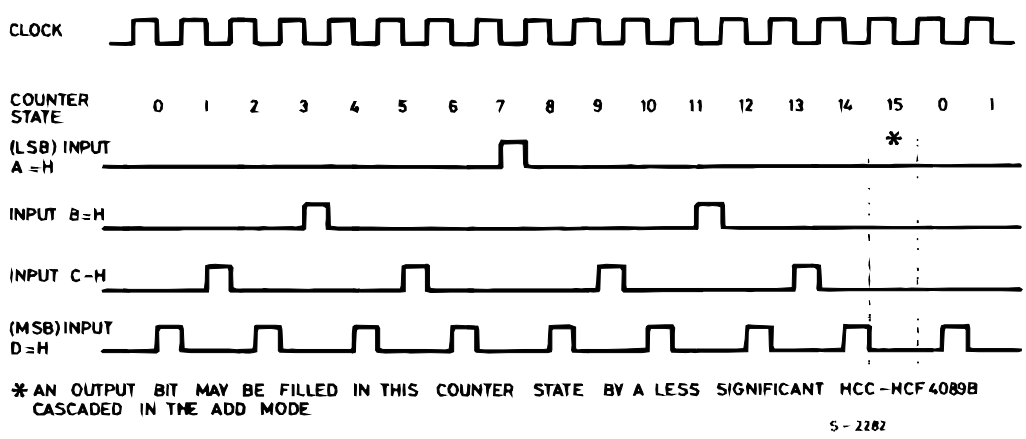
• : Depends on internal state of counter

*: Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time CLOCK to OUT	5			110	220	ns
		10			55	110	
		15			45	90	
t_{PHL} t_{PLH}	Propagation Delay Time CLOCK or STROBE to OUT	5			150	300	ns
		10			75	150	
		15			60	120	
t_{PHL} t_{PLH}	Propagation Delay Time CLOCK to INHIBIT High Level to Low Level	5			360	720	ns
		10			160	320	
		15			110	220	
t_{PHL} t_{PLH}	Propagation Delay Time LOW Level to HIGH Level	5			250	500	ns
		10			100	200	
		15			75	150	

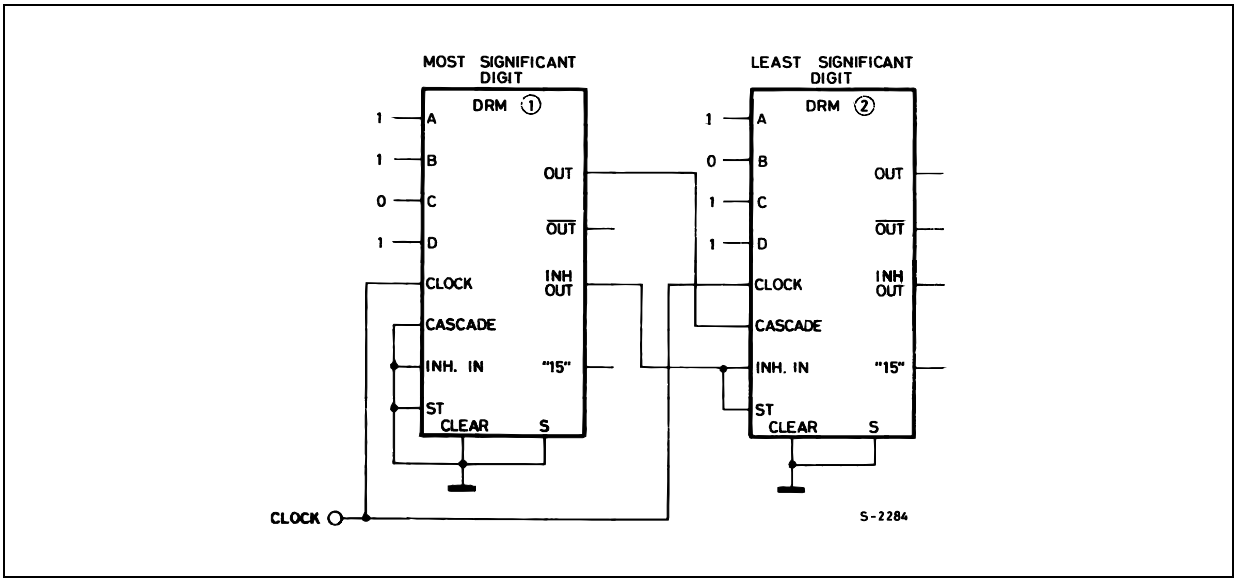
Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time CLEAR to OUT	5			380	760	ns
		10			175	350	
		15			130	260	
t_{PHL} t_{PLH}	Propagation Delay Time CLOCK to "9" or "15" OUT	5			300	600	ns
		10			125	250	
		15			90	180	
t_{PHL} t_{PLH}	Propagation Delay Time CASCADE to OUT	5			90	180	ns
		10			45	90	
		15			35	70	
t_{PHL} t_{PLH}	Propagation Delay Time INHIBIT IN to INHIBIT OUT	5			160	320	ns
		10			75	150	
		15			55	110	
t_{PHL} t_{PLH}	Propagation Delay Time SET to OUT	5			330	660	ns
		10			150	300	
		15			110	220	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
f_{CL}	Maximum Clock Frequency	5		1.2	2.4		MHz
		10		2.5	5		
		15		3.5	7		
t_W	Clock Pulse Width	5		330	165		ns
		10		170	85		
		15		100	50		
t_r, t_f	Clock Rise or Fall Time	5				15	µs
		10				15	
		15				15	
t_W	SET or CLEAR pulse Width	5		160	80		ns
		10		90	45		
		15		60	30		
t_{setup}	INHIBIT Input Set-Up Time, High Level to Low Level	5		100	50		ns
		10		40	20		
		15		20	10		
t_R	INHIBIT Input Removal Time	5		240	120		ns
		10		130	65		
		15		110	55		
t_R	Minimum SET Removal Time	5		150	75		ns
		10		80	40		
		15		50	25		
t_R	CLEAR Removal Time	5		60	30		ns
		10		40	20		
		15		30	15		

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

APPLICATION NOTES

For words of more than 4 bits, HCF4089B device may be cascaded in two different modes : an ADD mode and a MULTIPLY mode.

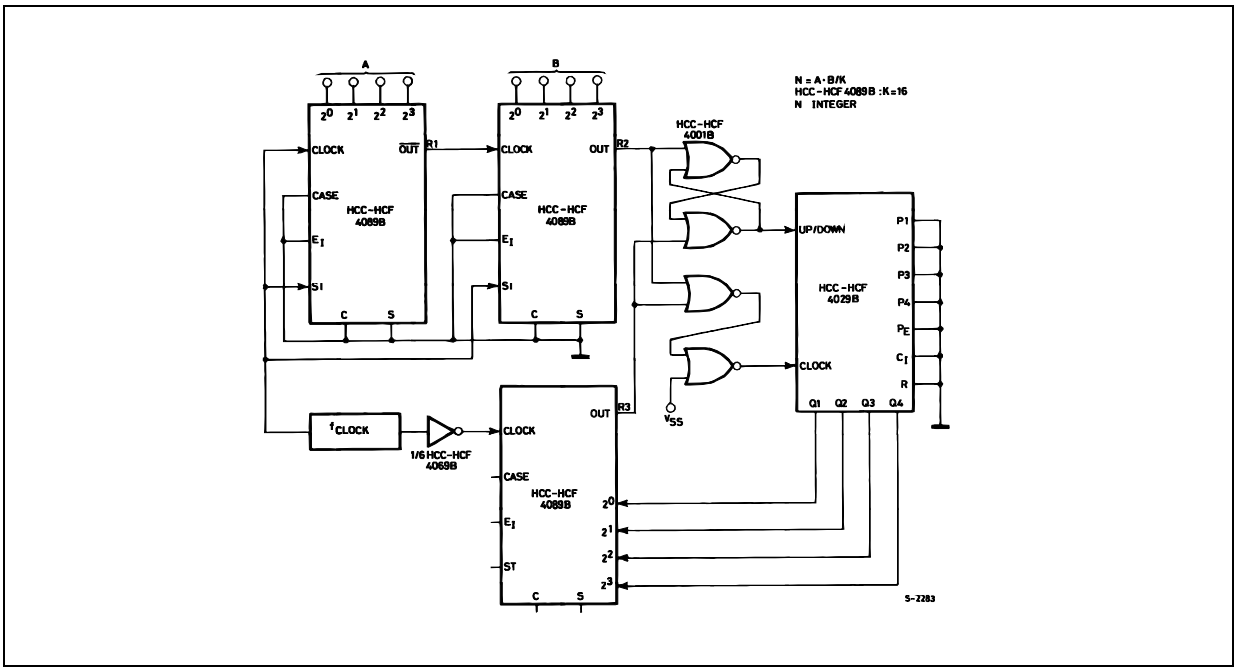
TWO HCF4089B'S CASCADED IN THE "ADD" MODE WITH A PRESET NUMBER OF 189



In the ADD mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the ADD mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of :

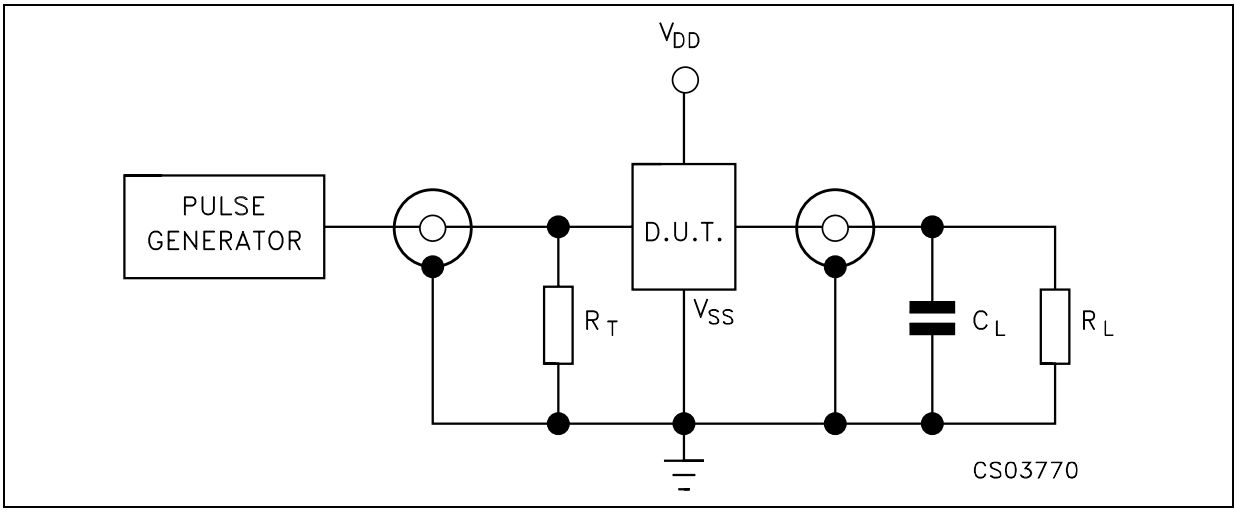
$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

TWO HCF4089B'S CASCADED IN THE "MULTIPLY" MODE FOR MULTIPLICATION OF TWO VARIABLES A AND B WITH LOOP CIRCUIT CONTROL



When the loop stabilities rate R2 = rate R3, thus $f_{clock}(\frac{A}{16} \bullet \frac{B}{16}) = f_{clock}(\frac{1}{16} \bullet \frac{N}{16})$ therefore N = AB

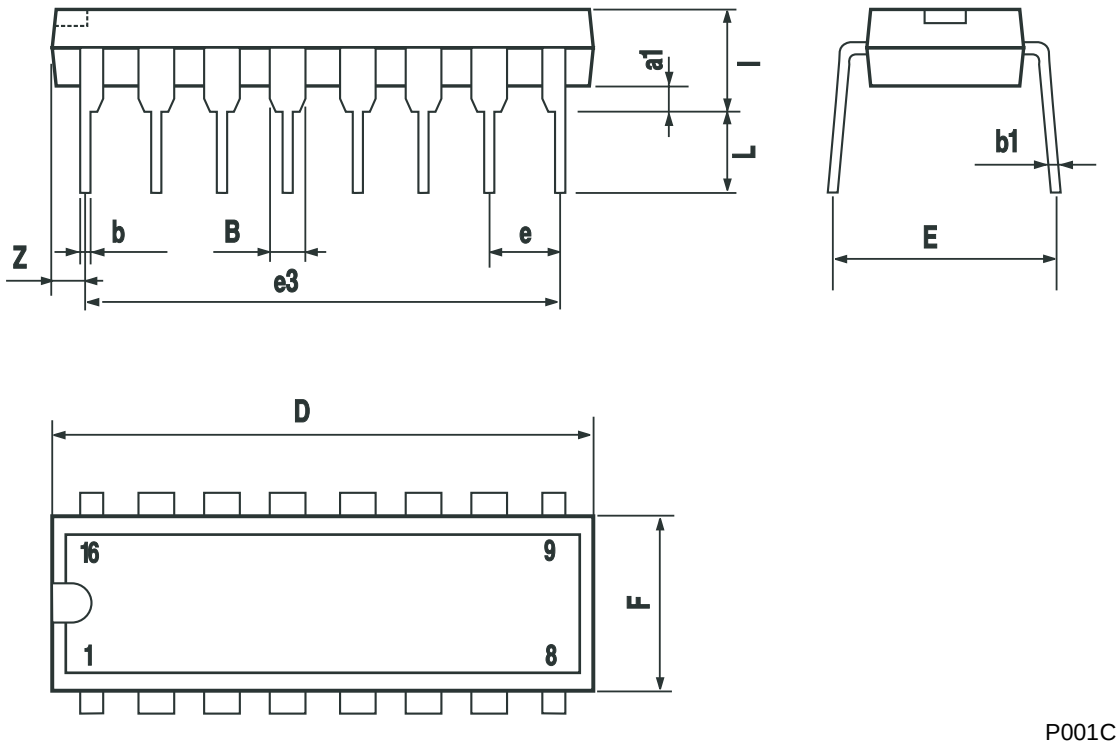
TEST CIRCUIT



C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Plastic DIP-16 (0.25) MECHANICAL DATA

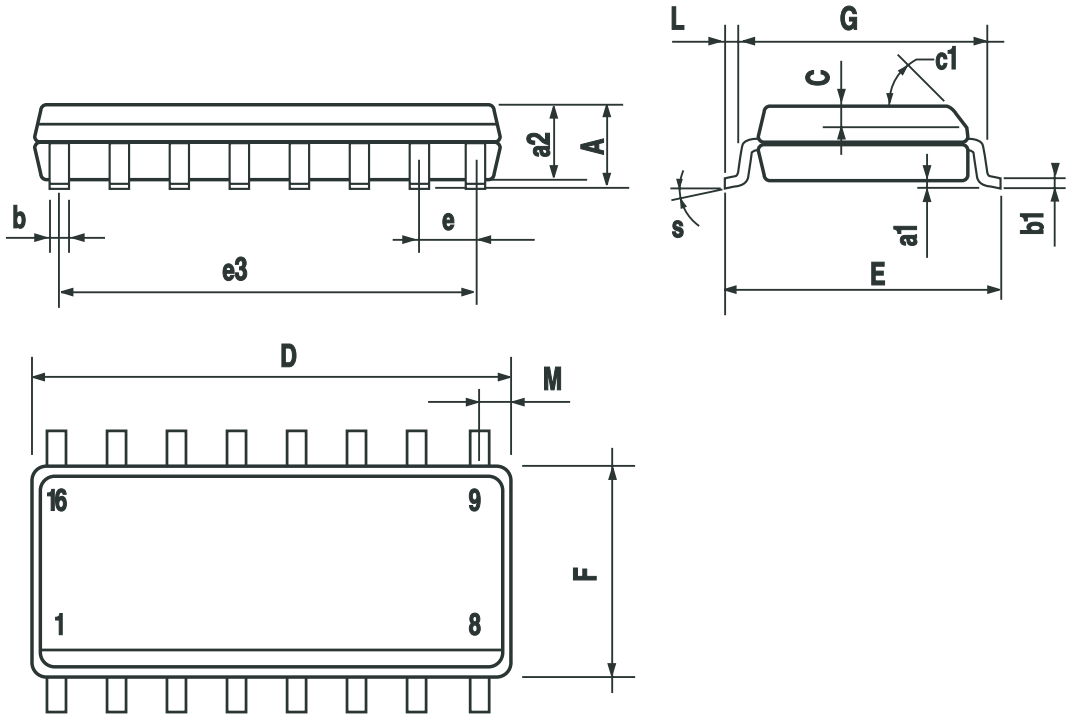
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H