



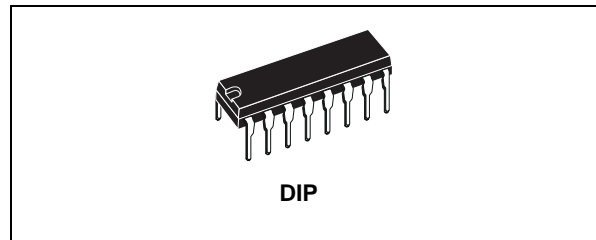
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

- MEDIUM SPEED OPERATION :
12 MHz (Typ.) at 10V
- FULLY STATIC OPERATION
- SYNCHRONOUS PARALLEL OR SERIAL OPERATION
- ASYNCHRONOUS MASTER RESET
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_l = 100\text{nA (MAX) AT } V_{DD} = 18\text{V } T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DESCRIPTION

HCF40194B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP packages.

HCF40194B is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the

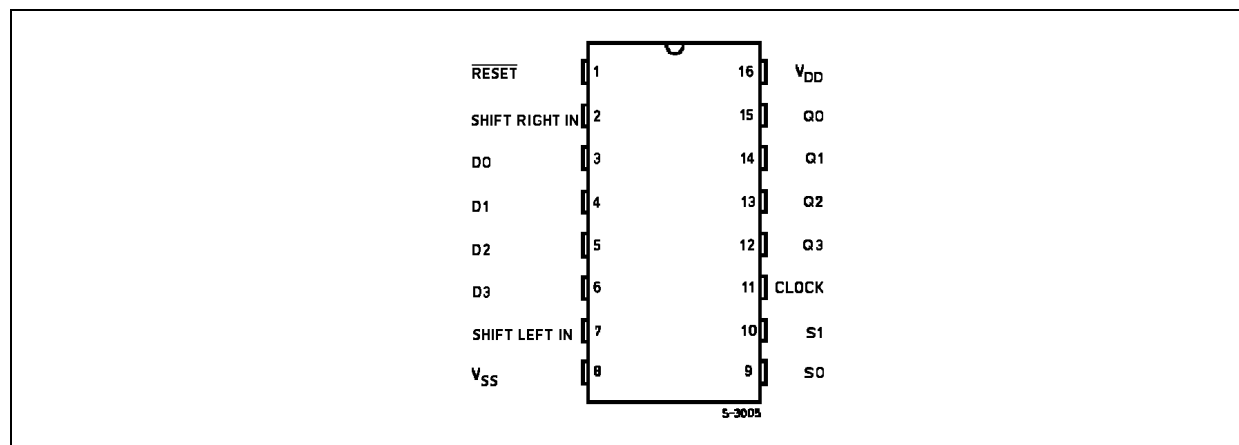


ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF40194BEY	

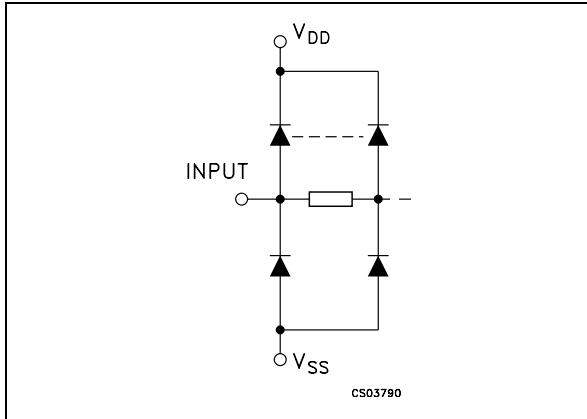
positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are synchronously accomplished on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the RESET input resets all stages and forces all outputs low. HCF40194B is similar to industry types 340194 and MC40194.

PIN CONNECTION



HCF40194B

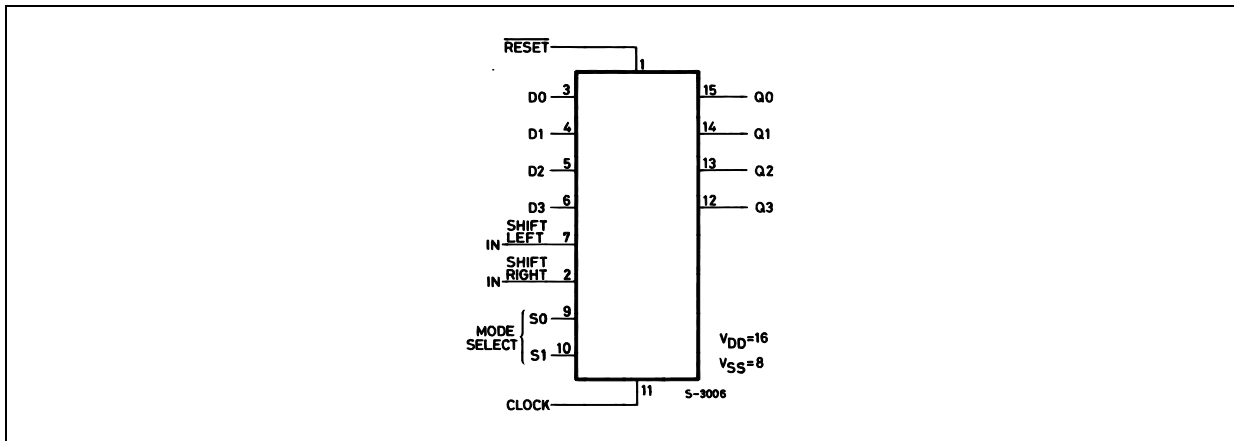
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	RESET	Reset Input
3, 4, 5, 6	D0 to D3	Inputs
15, 14, 13, 12	Q0 to Q3	Outputs
2	Shift Right IN	Shift Right Input
7	Shift Left IN	Shift Left Input
11	CLOCK	Clock Input
9, 10	S0, S1	Input (High)
8	V _{SS}	Negative Supply Voltage
16	V _{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM

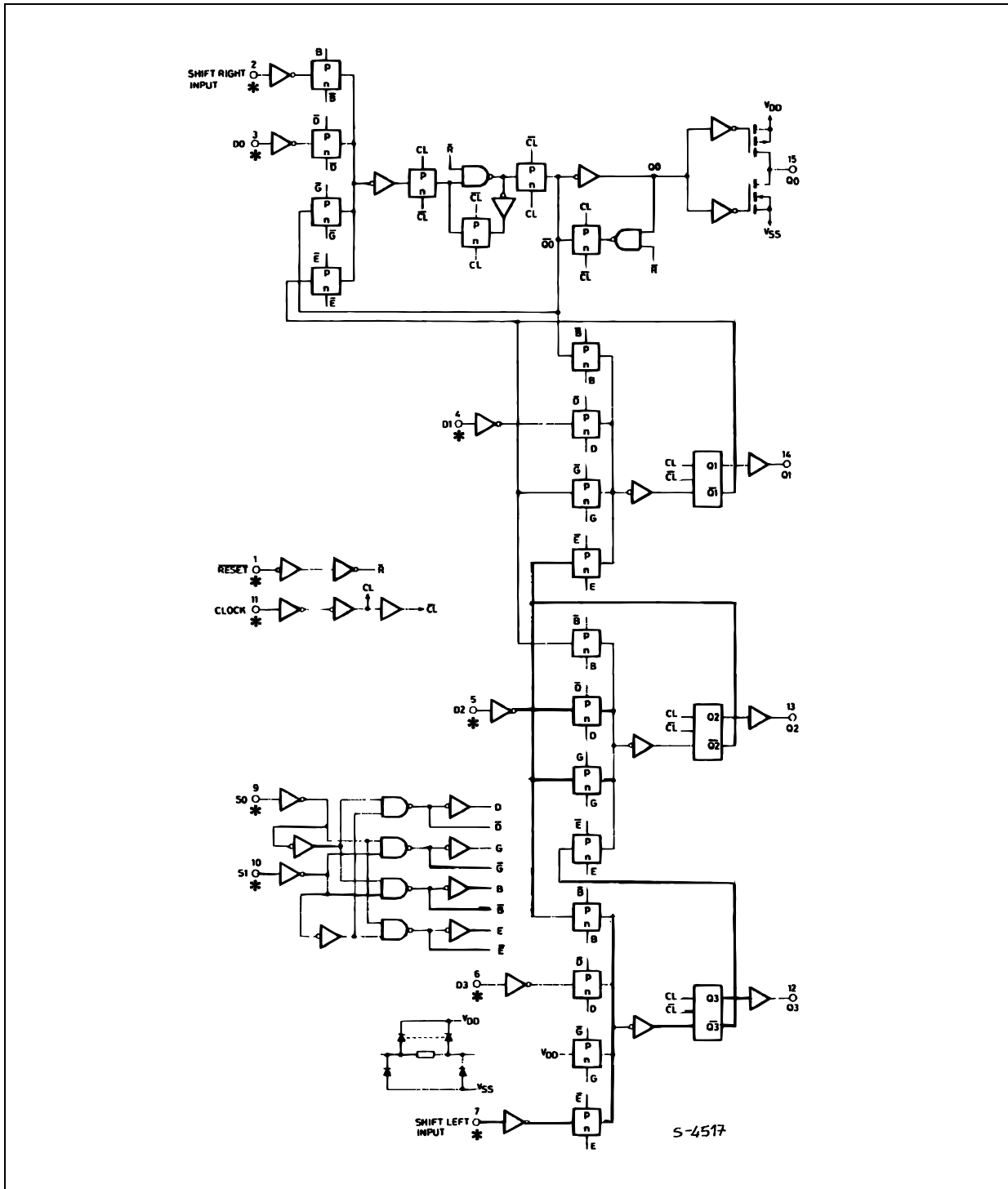


TRUTH TABLE

CLOCK	MODE SELECT		RESET	ACTION
	S0	S1		
X	L	L	H	NO CHANGE
	H	L	H	SHIFT RIGHT (Q0 toward Q3)
	L	H	H	SHIFT LEFT (Q3 toward Q0)
	H	H	H	PARALLEL LOAD
X	X	X	L	RESET

X : Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V _I (V)	V _O (V)	I _{OL} (μ A)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μ A
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	± 0.1		± 1		± 1	μ A
C _I	Input Capacitance		Any Input				5	7.5					pF

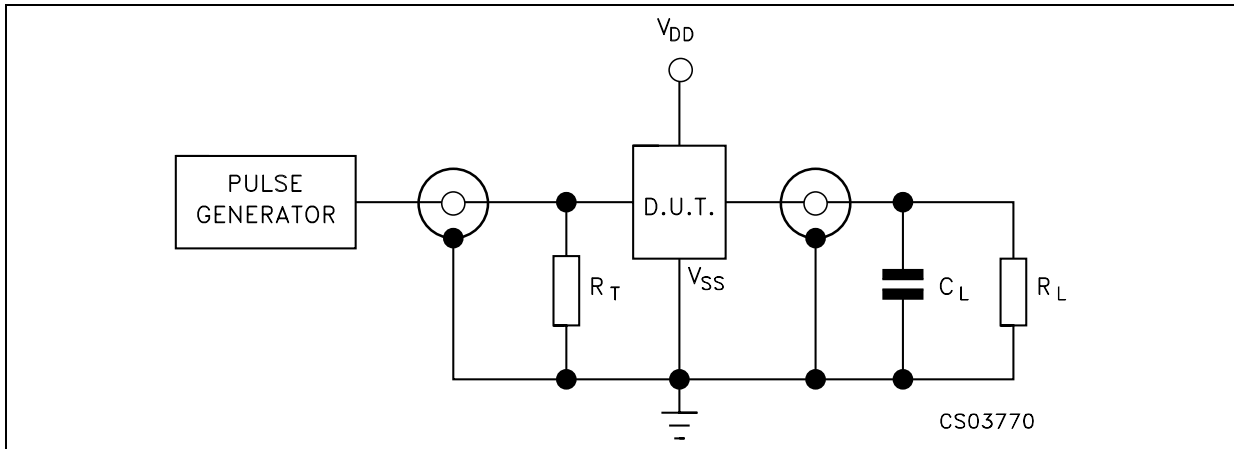
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

HCF40194B

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

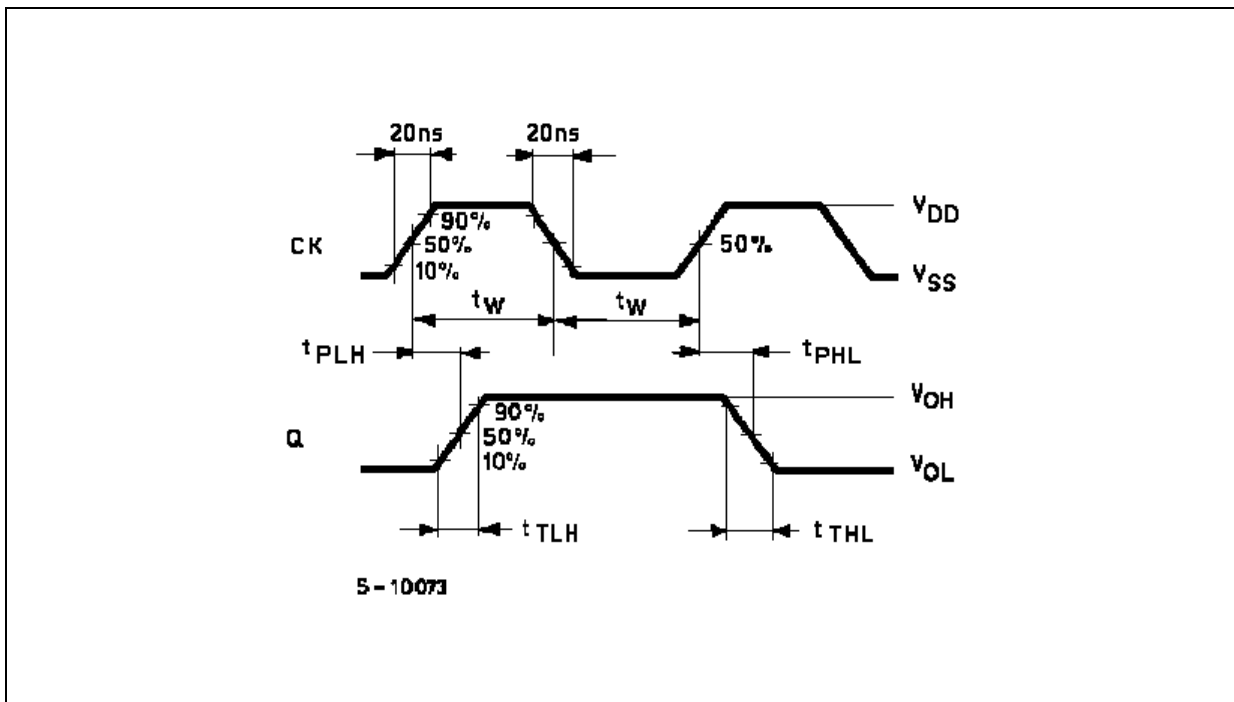
Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Q	5			220	440	ns
		10			100	200	
		15			70	140	
t_{PHZ}		5			45	90	ns
		10			25	50	
		15			20	40	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{setup}	Setup Time D0, D3, SR, SL to Clock	5			80	100	ns
		10			35	70	
		15			20	50	
	SO, S1 to Clock	5			200	400	ns
		10			110	220	
		15			65	130	
t_{hold}	Hold Time D0, D3, SR, SL to Clock	5			-65	0	ns
		10			-25	0	
		15			-15	0	
	SO, S1 to Clock	5			-170	0	ns
		10			-95	0	
		15			-55	0	
t_W	Clock Pulse Width	5			90	180	ns
		10			40	180	
		15			25	50	
f_{CL}	Clock Input Frequency	5		3	6		MHz
		10		6	12		
		15		8	15		
t_r , t_f	Clock Input Rise or Fall Time	5				1000	μs
		10				100	
		15				100	
t_W	Reset Pulse Width	5			150	300	ns
		10			100	200	
		15			70	140	
t_{PRHL}	Propagation Delay Reset	5			230	460	ns
		10			90	180	
		15			65	130	

TEST CIRCUIT

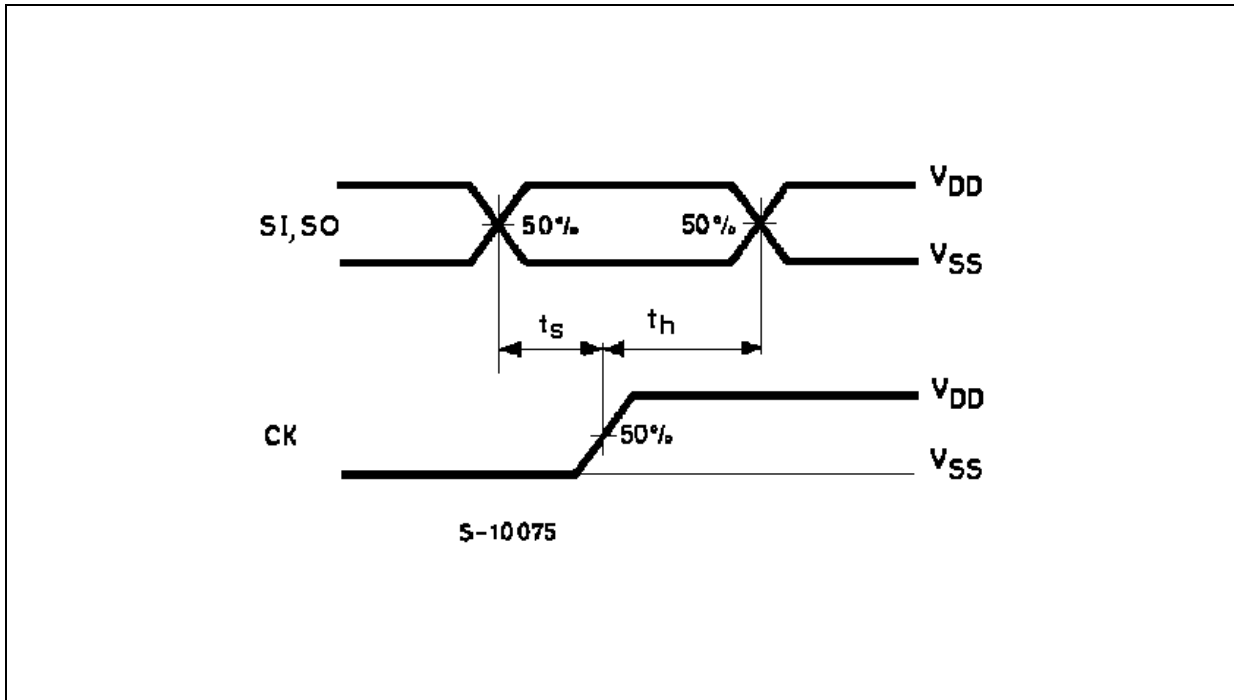


$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 200\text{K}\Omega$
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

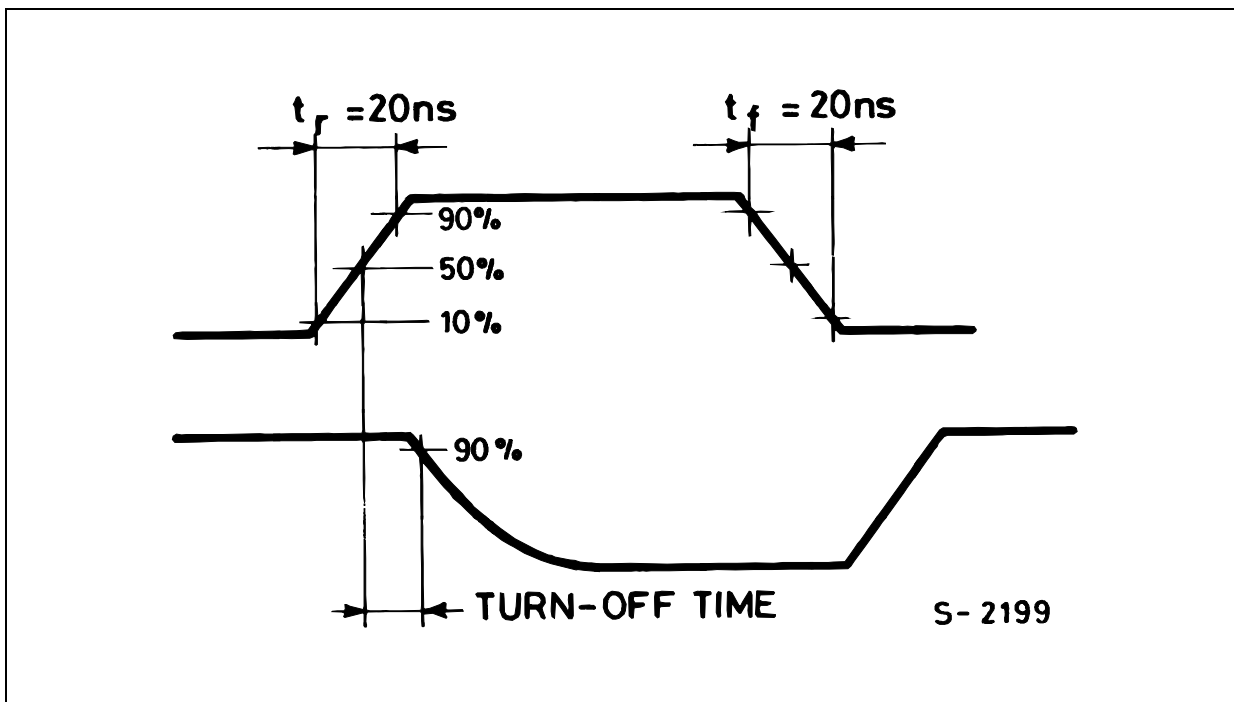
WAVEFORM 1 : CK TO Q PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



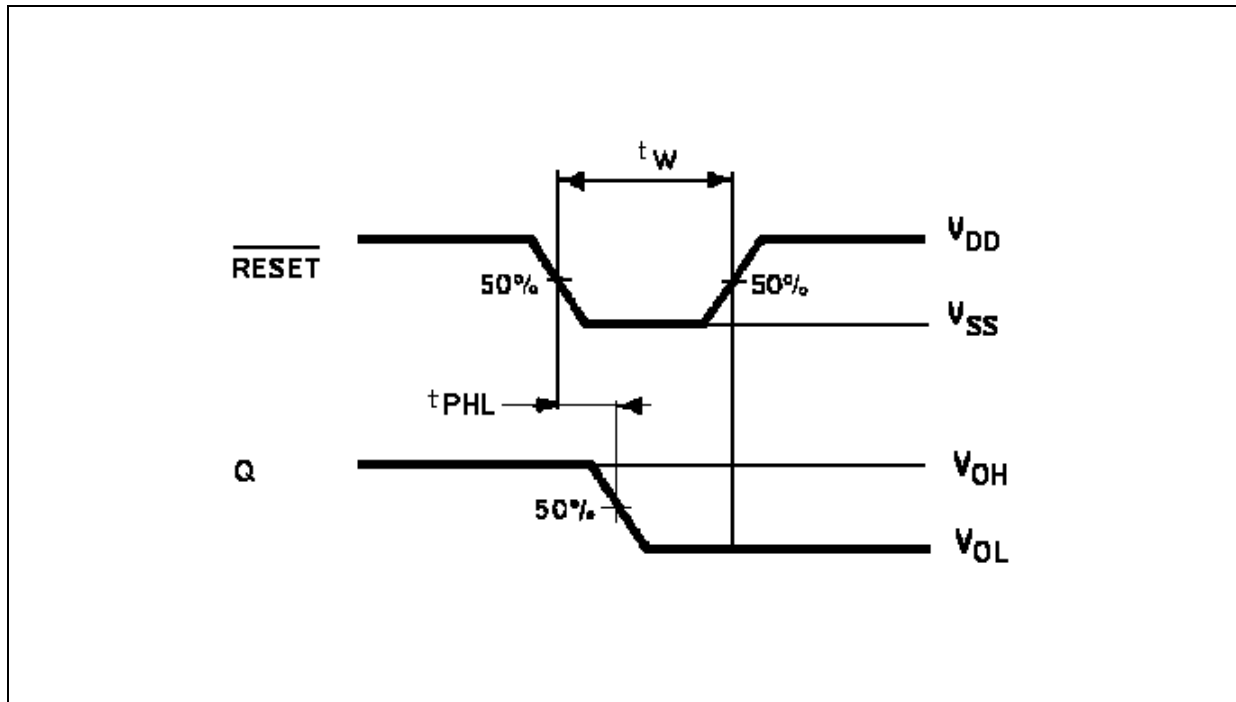
WAVEFORM 2 : SI, SO SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 3 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)

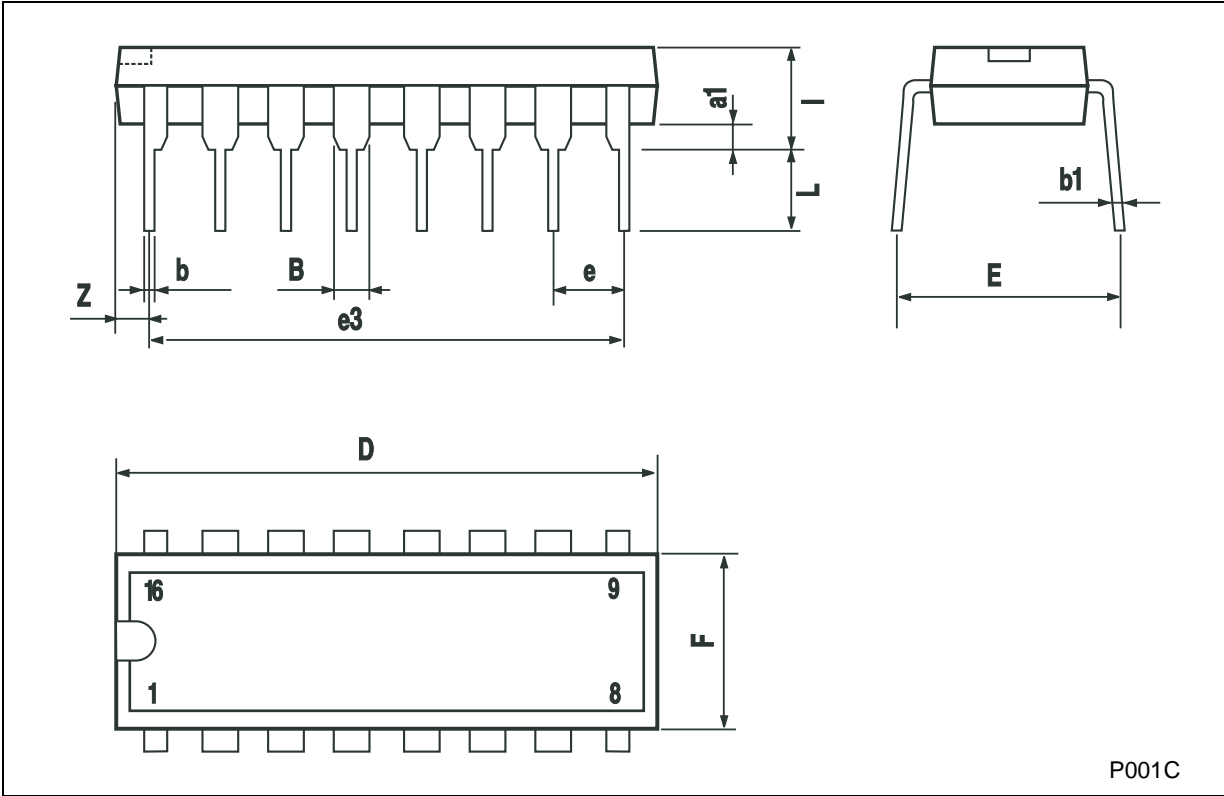


WAVEFORM 4 : PROPAGATION DELAY TIME, $\overline{\text{RESET}}$ MINIMUM PULSE WIDTH ($f=1\text{MHz}$; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C



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