ADC08031,ADC08032,ADC08034,ADC08038

ADC08031/ADC08032/ADC08034/ADC08038 8-Bit High-Speed Serial I/O A/D Converters with Multiplexer Options, Voltage Reference, and Track/Hold Function

TEXAS INSTRUMENTS

Literature Number: SNAS062B

National Semiconductor

OBSOLETE

January 15, 2007

ADC08031/ADC08032/ADC08034/ADC08038 8-Bit High-Speed Serial I/O A/D Converters with Multiplexer Options, Voltage Reference, and Track/Hold Function

General Description

The ADC08031/ADC08032/ADC08034/ADC08038 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of controllers, and can easily interface with standard shift registers or microprocessors.

The ADC08034 and ADC08038 provide a 2.6V band-gap derived reference. For devices offering guaranteed voltage reference performance over temperature see ADC08131, ADC08134 and ADC08138.

A track/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. In addition, input voltage spans as small as 1V can be accommodated.

Applications

- Digitizing automotive sensors
- Process control monitoring
- Remote sensing in noisy environments
- Instrumentation
- Test systems
- Embedded diagnostics

Features

- Serial digital data link requires few I/O pins
- Analog input track/hold function
- 2-, 4-, or 8-channel input multiplexer options with address logic
- 0V to 5V analog input range with single 5V power supply
- No zero or full scale adjustment required
- TTL/CMOS input/output compatible
- On chip 2.6V band-gap reference
- 0.3″ standard width 8-, 14-, or 20-pin DIP package
- 14-, 20-pin small-outline packages

Key Specifications

- Resolution: 8 bits
- Conversion time (f_C = 1 MHz): 8µs (max)
- Power dissipation: 20mW (max)
- Single supply: $5V_{DC}$ (±5%)
- Total unadjusted error: ±½ LSB and ±1LSB
- No missing codes over temperature

Ordering Information

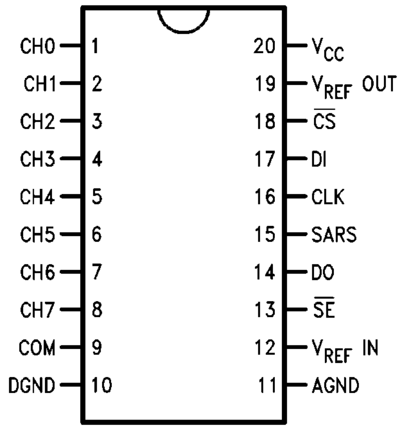
Industrial (−40°C ≤ T_A ≤ +85°C)	Package
ADC08031CIN	N08E
ADC08038CIN	N20A
ADC08031CIWM, ADC08032CIWM, ADC08034CIWM	M14B
ADC08038CIWM	M20B

This device is obsolete in all packages.

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

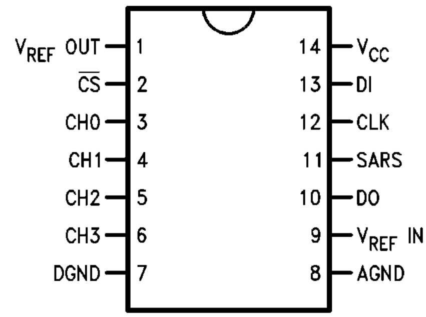
Connection Diagrams

ADC08038



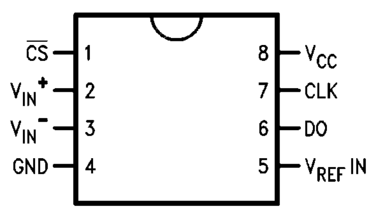
1055502

ADC08034



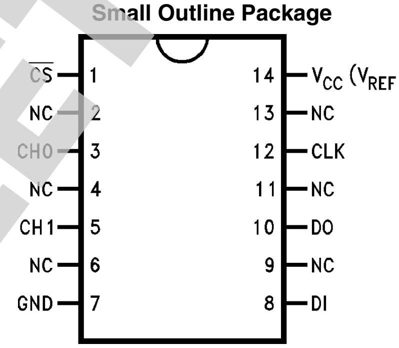
1055503

ADC08031
Dual-In-Line Package



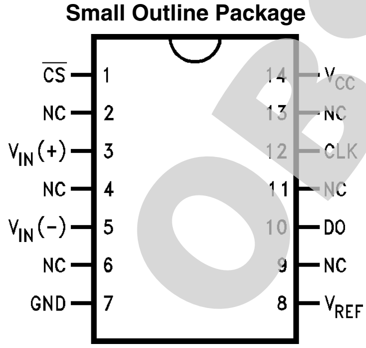
1055505

ADC08032
Small Outline Package



1055530

ADC08031
Small Outline Package



1055531

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.5V
Voltage at Inputs and Outputs	−0.3V to V_{CC} + 0.3V
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Power Dissipation at T_A = 25°C (Note 5)	800 mW
ESD Susceptibility (Note 6)	1500V
Soldering Information	
N Package (10 sec.)	235°C
SO Package:	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.) (Note 7)	220°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 2, 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC08031BIN, ADC08031CIN, ADC08032BIN, ADC08032CIN, ADC08034BIN, ADC08034CIN, ADC08038BIN, ADC08038CIN, ADC08031BIWM, ADC08032BIWM, ADC08034BIWM, ADC08038BIWM ADC08031CIWM, ADC08032CIWM, ADC08034CIWM, ADC08038CIWM	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_{CC})	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for $V_{CC} = V_{REF} = +5\ V_{DC}$, and f_{CLK} = 1 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
	Total Unadjusted Error	(Note 10)			
	BIN, BIWM			**±½**	LSB (max)
	CIN, CIWM			**±1**	LSB (max)
	Differential Linearity			**8**	Bits (min)
R_{REF}	Reference Input Resistance	(Note 11)	3.5		kΩ
				1.3	kΩ (min)
				6.0	kΩ (max)
V_{IN}	Analog Input Voltage	(Note 12)		**(V_{CC} + 0.05)**	V (max)
				(GND – 0.05)	V (min)
	DC Common-Mode Error			±¼	LSB (max)
	Power Supply Sensitivity	V_{CC} = 5V ±5%, V_{REF} = 4.75V		**±¼**	LSB (max)
	On Channel Leakage Current (Note 13)	On Channel = 5V, Off Channel = 0V		0.2 **1**	µA (max)
		On Channel = 0V, Off Channel = 5V		−0.2 **−1**	µA (max)
	Off Channel Leakage Current (Note 13)	On Channel = 5V, Off Channel = 0V		−0.2 **−1**	µA (max)
		On Channel = 0V, Off Channel = 5V		0.2 **1**	µA (max)
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$	Logical “1” Input Voltage	V_{CC} = 5.25V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_{CC} = 4.75V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 5.0V		**1**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V		**−1**	µA (max)

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
$V_{OUT(1)}$	Logical “1” Output Voltage	V_{CC} = 4.75V: I_{OUT} = −360 µA I_{OUT} = −10 µA		 **2.4** **4.5**	 V (min) V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	V_{OUT} = 0V V_{OUT} = 5V		**–3.0** **3.0**	µA (max) µA (max)
I_{SOURCE}	Output Source Current	V_{OUT} = 0V		**–6.5**	mA (min)
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}		**8.0**	mA (min)
I_{CC}	Supply Current ADC08031, ADC08034, and ADC08038 ADC08032 (Note 16)	$\overline{CS}$ = HIGH		**3.0** **7.0**	mA (max) mA (max)
REFERENCE CHARACTERISTICS					
$V_{REF}OUT$	Nominal Reference Output	$V_{REF}OUT$ Option Available Only on ADC08034 and ADC08038	2.6		V

Electrical Characteristics

The following specifications apply for $V_{CC} = V_{REF} = +5\ V_{DC}$, and $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
f_{CLK}	Clock Frequency		10	 **1**	kHz (min) MHz (max)
	Clock Duty Cycle (Note 14)			**40** **60**	% (min) % (max)
T_C	Conversion Time (Not Including MUX Addressing Time)	f_{CLK} = 1 MHz		**8** **8**	$1/f_{CLK}$ (max) µs (max)
t_{CA}	Acquisition Time			**½**	$1/f_{CLK}$(max)
t_{SELECT}	CLK High while $\overline{CS}$ is High		50		ns
t_{SET-UP}	$\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge			**25**	ns (min)
t_{HOLD}	Data Input Valid after CLK Rising Edge			**20**	ns (min)
t_{pd1}, t_{pd0}	CLK Falling Edge to Output Data Valid (Note 15)	C_L = 100 pF: Data MSB First Data LSB First		 **250** **200**	 ns (max) ns (max)
t_{1H}, t_{0H}	TRI-STATE Delay from Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	C_L = 10 pF, R_L = 10 kΩ (see TRI-STATE Test Circuits)	50		ns
		C_L = 100 pF, R_L = 2 kΩ		**180**	ns (max)
C_{IN}	Capacitance of Logic Inputs		5		pF
C_{OUT}	Capacitance of Logic Outputs		5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to AGND = DGND = 0 V_{DC}, unless otherwise specified.

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Note 4: When the input voltage V_{IN} at any pin exceeds the power supplies (V_{IN} < (AGND or DGND) or $V_{IN} > V_{CC}$) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For these devices, T_{JMAX} = 125°C. The typical thermal resistances (θ_{JA}) of these parts when board mounted follow: ADC08031 and ADC08032 with BIN and CIN suffixes 120°C/W, ADC08038 with CIN suffix 80°C/W. ADC08031 with CIWM suffix 140°C/W, ADC08032 140°C/W, ADC08034 140°C/W, ADC08038 with CIWM suffix 91°C/W.

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or Linear Data Book section "Surface Mount" for other methods of soldering surface mount devices.

Note 8: Typical figures are at T_J = 25°C and represent the most likely parametric norm.

Note 9: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Total unadjusted error includes offset, full-scale, linearity, multiplexer.

Note 11: Cannot be tested for the ADC08032.

Note 12: For $V_{IN(-)} \geq V_{IN(+)}$ the digital code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. During testing at low V_{CC} levels (e.g., 4.5V), high level analog inputs (e.g., 5V) can cause an input diode to conduct, especially at elevated temperatures, which will cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode; this means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. Exceeding this range on an unselected channel will corrupt the reading of a selected channel. Achievement of an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 13: Channel leakage current is measured after a single-ended channel is selected and the clock is turned off. For off channel leakage current the following two cases are considered: one, with the selected channel tied high (5 V_{DC}) and the remaining seven off channels tied low (0 V_{DC}), total current flow through the off channels is measured; two, with the selected channel tied low and the off channels tied high, total current flow through the off channels is again measured. The two cases considered for determining on channel leakage current are the same except total current flow through the selected channel is measured.

Note 14: A 40% to 60% duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits the minimum time the clock is high or low must be at least 450 ns. The maximum time the clock can be high or low is 100 µs.

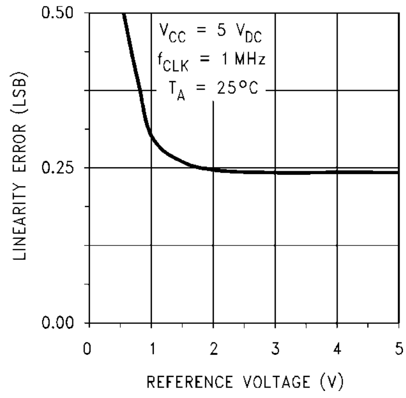
Note 15: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Note 16: For the ADC08032 V_{REF}IN is internally tied to V_{CC}, therefore, for the ADC08032 reference current is included in the supply current.

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

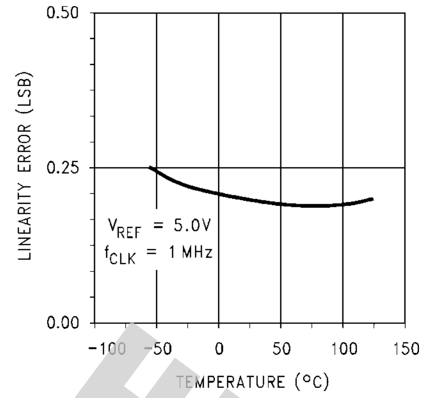
Typical Performance Characteristics

Linearity Error vs. Reference Voltage



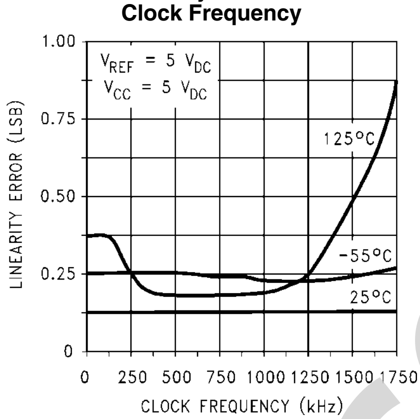
1055532

Linearity Error vs. Temperature



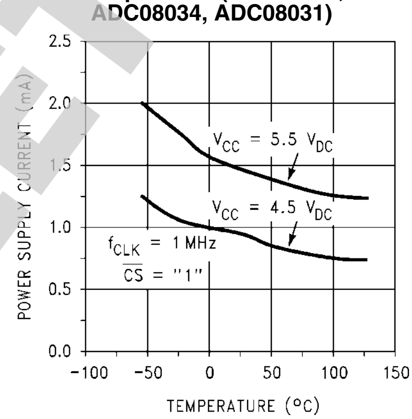
1055533

Linearity Error vs. Clock Frequency



1055534

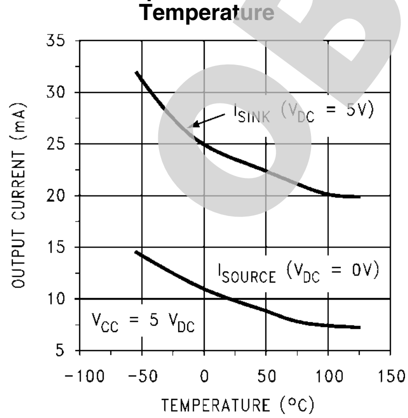
Power Supply Current vs. Temperature (ADC08038, ADC08034, ADC08031)



1055535

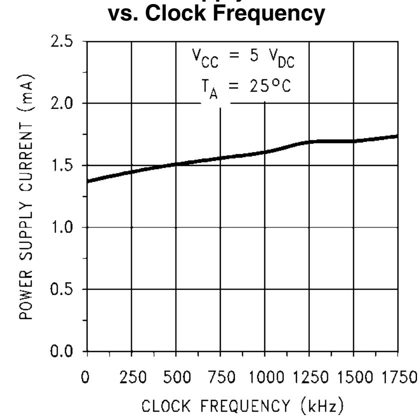
Note: For ADC08032 add I_{REF}

Output Current vs. Temperature



1055536

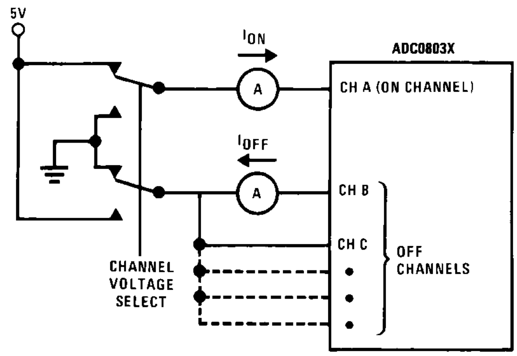
Power Supply Current vs. Clock Frequency



1055537

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

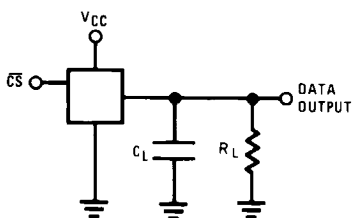
Leakage Current Test Circuit



1055507

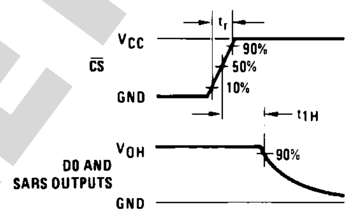
TRI-STATE Test Circuits and Waveforms

t_{1H}



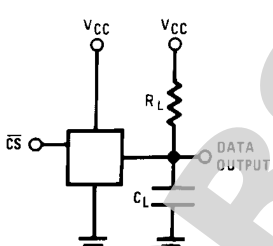
1055538

t_{1H}



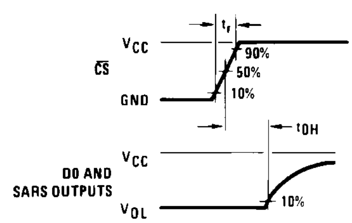
1055539

t_{0H}



1055540

t_{0H}

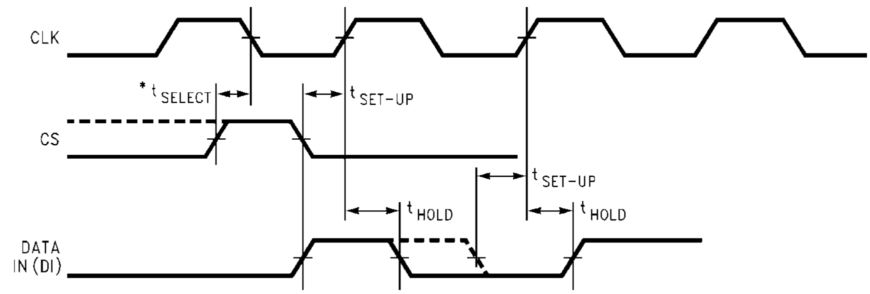


1055541

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Timing Diagrams

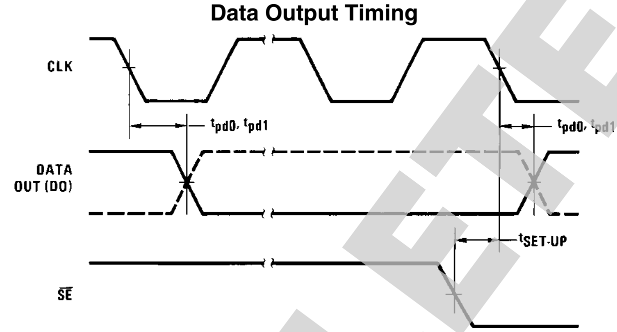
Data Input Timing



1055510

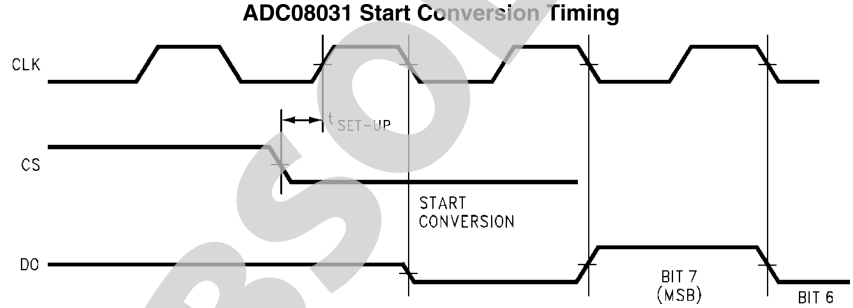
*To reset these devices, CLK and $\overline{CS}$ must be simultaneously high for a period of t_{SELECT} or greater. Otherwise these devices are compatible with industry standards ADC0831/2/4/8.

Data Output Timing



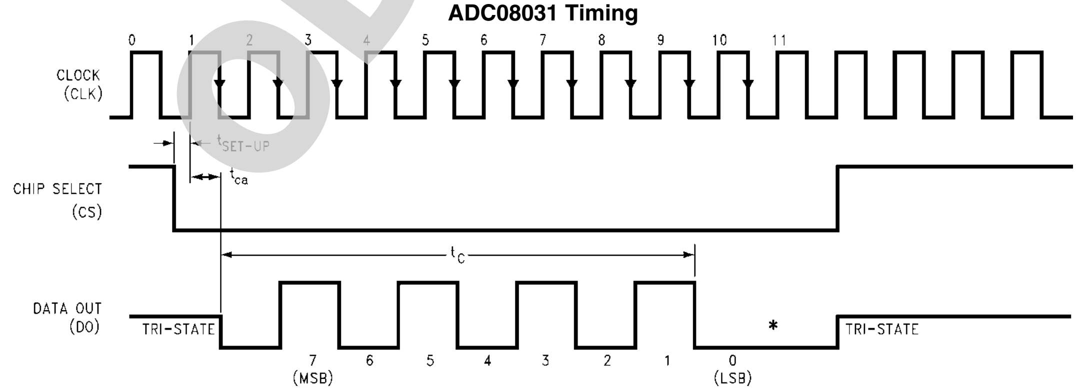
1055511

ADC08031 Start Conversion Timing



1055512

ADC08031 Timing



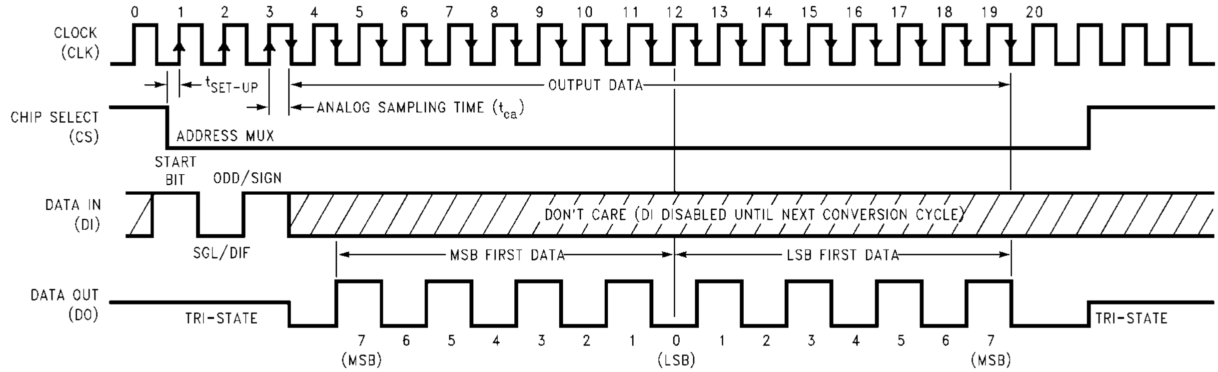
1055513

*LSB first output not available on ADC08031.

LSB information is maintained for remainder of clock periods until $\overline{CS}$ goes high.

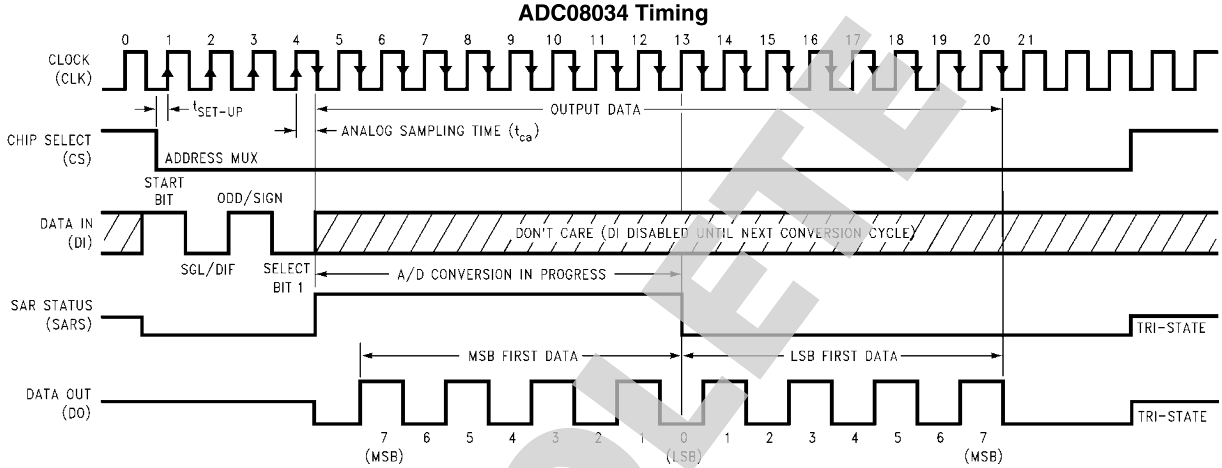
10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

ADC08032 Timing



1055514

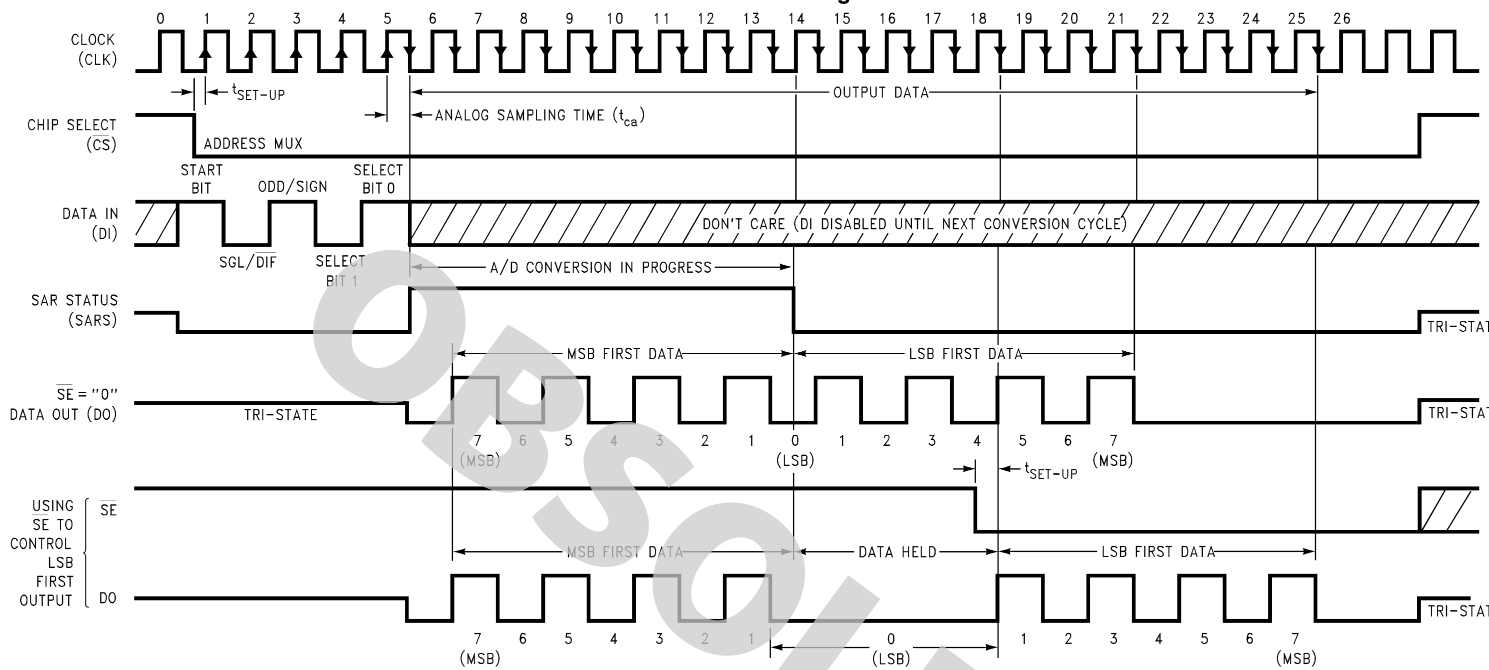
ADC08034 Timing



1055515

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

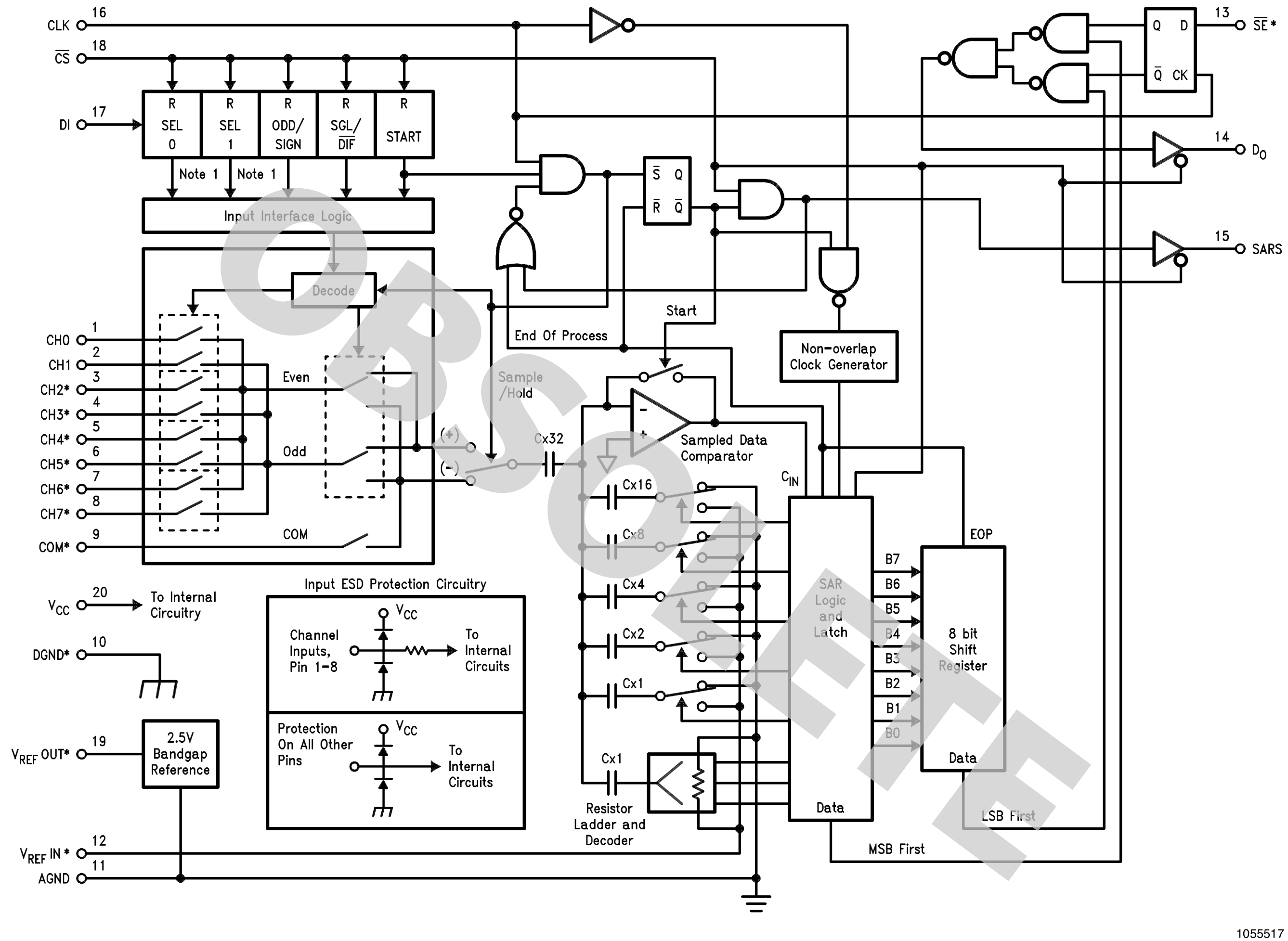
ADC08038 Timing



*Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

ADC08038 Functional Block Diagram



*Some of these functions/pins are not available with other options.

For the ADC08034, the “SEL 1” Flip-Flop is bypassed, for the ADC08032, both “SEL 0” and “SEL 1” Flip-Flops are bypassed.

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a comparator structure with built-in sample-and-hold which provides for a differential analog input to be converted by a successive-approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair indicates which line the converter expects to be the most positive. If the assigned "+" input voltage is less than the "−" input voltage the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or pseudo-differential (which will convert the difference between the voltage at any analog input and a common terminal) operation. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. Differential inputs are restricted to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the polarity may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC08031 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line (COM) on the ADC08038 can be used as a pseudo-differential input. In this mode the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply applications where the analog circuity may be biased up to a potential other than ground and the output signals are all referred to this potential.

TABLE 1. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC08031	1	1	8
ADC08032	2	1	8
ADC08034	4	2	14
ADC08038	8	4	20

TABLE 2. MUX Addressing: ADC08038

Single-Ended MUX Mode

MUX Address					Analog Single-Ended Channel #								
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	1	0	0	0	+								−
1	1	0	0	1			+						−
1	1	0	1	0					+				−
1	1	0	1	1							+		−
1	1	1	0	0		+							−
1	1	1	0	1				+					−
1	1	1	1	0						+			−
1	1	1	1	1								+	−

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

TABLE 3. MUX Addressing: ADC08038

Differential MUX Mode													
MUX Address					Analog Differential Channel-Pair #								
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT		0		1		2		3		
			1	0	0	1	2	3	4	5	6	7
1	0	0	0	0	+	–						
1	0	0	0	1			+	–				
1	0	0	1	0					+	–		
1	0	0	1	1							+	–
1	0	1	0	0	–	+						
1	0	1	0	1			–	+				
1	0	1	1	0					–	+		
1	0	1	1	1							–	+

TABLE 4. MUX Addressing: ADC08034

Single-Ended MUX Mode							
MUX Address				Channel #			
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT 1	0	1	2	3
1	1	0	0	+			
1	1	0	1			+	
1	1	1	0		+		
1	1	1	1				+
COM is internally tied to AGND							

MUX Addressing: ADC08032

Single-Ended MUX Mode				
MUX Address			Channel #	
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	0	1
1	1	0	+	
1	1	1		+
COM is internally tied to AGND				

Differential MUX Mode							
MUX Address				Channel #			
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	SELECT 1	0	1	2	3
1	0	0	0	+	–		
1	0	0	1			+	–
1	0	1	0	–	+		
1	0	1	1			–	+

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Differential MUX Mode				
MUX Address			Channel #	
START	SGL/ $\overline{\text{DIF}}$	ODD/ SIGN	0	1
1	0	0	+	−
1	0	1	−	+

Since the input configuration is under software control, it can be modified as required before each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50mV below ground to 50mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows many functions to be included in a small package and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate timing diagram is shown for each device.

1. A conversion is initiated by pulling the $\overline{\text{CS}}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.
2. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.
3. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SARS line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).
4. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.
5. During the conversion the output of the SAR comparator indicates whether the analog input is greater than (high) or less than (low) a series of successive voltages generated internally from a ratioed capacitor array (first 5 bits) and a resistor ladder (last 3 bits). After each comparison the comparator's output is shipped to the DO line on the falling edge of CLK. This data is the result of the conversion being shifted out (with the MSB first) and can be read by the processor immediately.
6. After 8 clock periods the conversion is completed. The SARS line returns low to indicate this ½ clock cycle later.
7. The stored data in the successive approximation register is loaded into an internal shift register. If the programmer prefers the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{\text{SE}}$) control line]. On the ADC08038 the $\overline{\text{SE}}$ line is brought out and if held high the value of the LSB remains valid on the DO line. When $\overline{\text{SE}}$ is forced low the data is clocked out LSB first. On devices which do not include the $\overline{\text{SE}}$ control line, the data, LSB first, is automatically shifted out the DO line after the MSB first data stream. The DO line then goes low and stays low until $\overline{\text{CS}}$ is returned high. The ADC08031 is an exception in that its data is only output in MSB first format.
8. All internal registers are cleared when the $\overline{\text{CS}}$ line is high and the t_{SELECT} requirement is met. See Data Input Timing under Timing Diagrams. If another conversion is desired $\overline{\text{CS}}$ must make a high to low transition followed by address information.

   The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

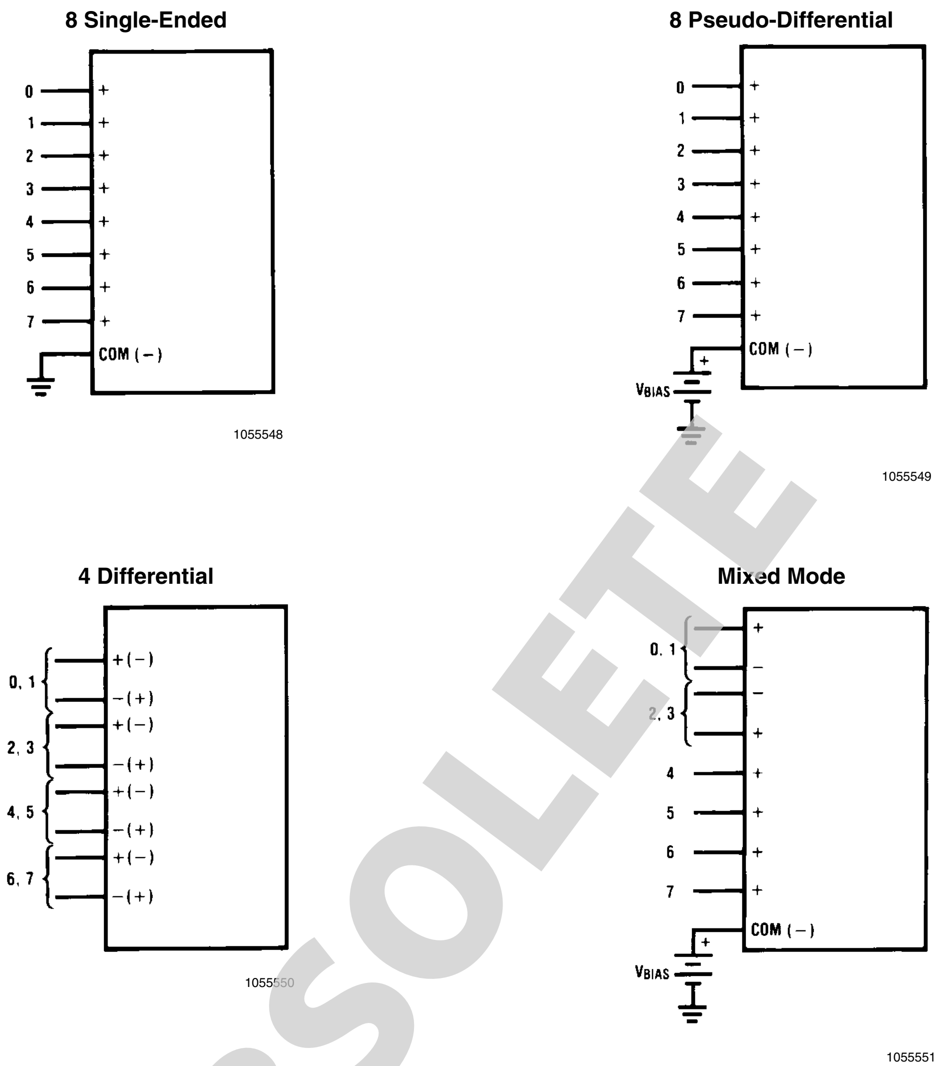


FIGURE 1. Analog Input Multiplexer Options for the ADC08038

3.0 REFERENCE CONSIDERATIONS

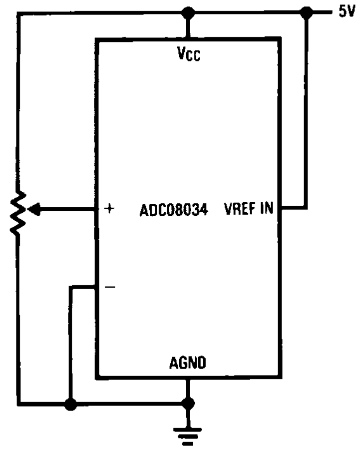
The voltage applied to the reference input on these converters, V_{REF}IN, defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$ over which the 256 possible output codes apply. The devices can be used either in ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance which can be as low as 1.3kΩ. This pin is the top of a resistor divider string and capacitor array used for the successive approximation conversion.

In a ratiometric system the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF}IN pin can be tied to V_{CC} (done internally on the ADC08032). This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

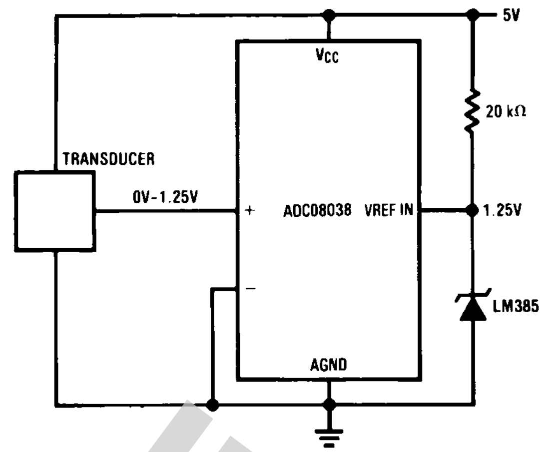
For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. For the ADC08034 and the ADC08038 a band-gap derived reference voltage of 2.6V (Note 8) is tied to V_{REF}OUT. This can be tied back to V_{REF}IN. Bypassing V_{REF}OUT with a 100µF capacitor is recommended. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF/}$256).

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10



a) Ratiometric



b) Absolute with a Reduced Span

FIGURE 2. Reference Examples

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "–" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "–" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK} is the A/D clock frequency.

For a 60Hz common-mode signal to generate a ¼ LSB error (≈5mV) with the converter running at 250kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Source resistance limitation is important with regard to the DC leakage currents of the input multiplexer. Bypass capacitors should not be used if the source resistance is greater than 1kΩ. The worst-case leakage current of ±1µA over temperature will create a 1mV input error with a 1kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (–) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (–) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for $V_{REF} = 5.000V_{DC}$).

5.2 Full Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF}IN input (or V_{CC} for the ADC08032) for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/ 256) is applied to selected "+" input and the zero reference voltage at the corresponding "–" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN} (–) voltage applied] by forcing a voltage to the V_{IN} (+) input which is given by:

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

$$V_{IN}\,(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

and

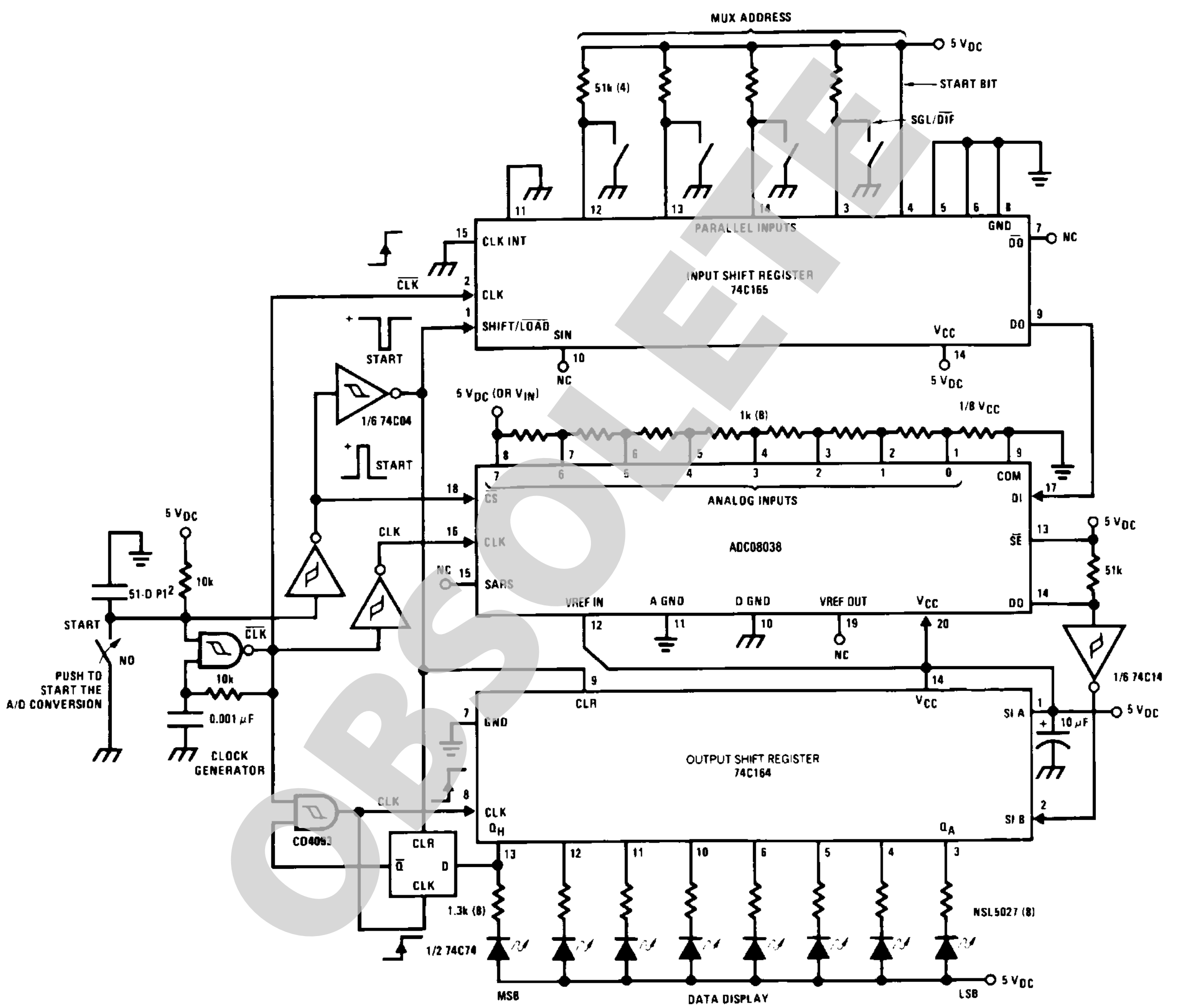
V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The V_{REF}IN (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

Applications

A “Stand-Alone” Hook-Up for ADC08038 Evaluation



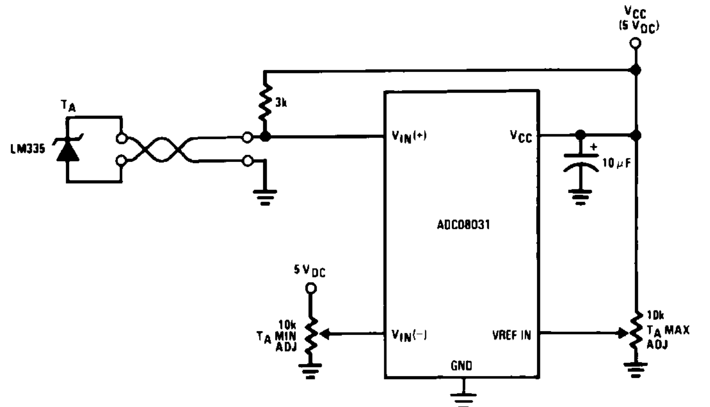
1055544

*Pinouts shown for ADC08038.

For all other products tie to pin functions as shown.

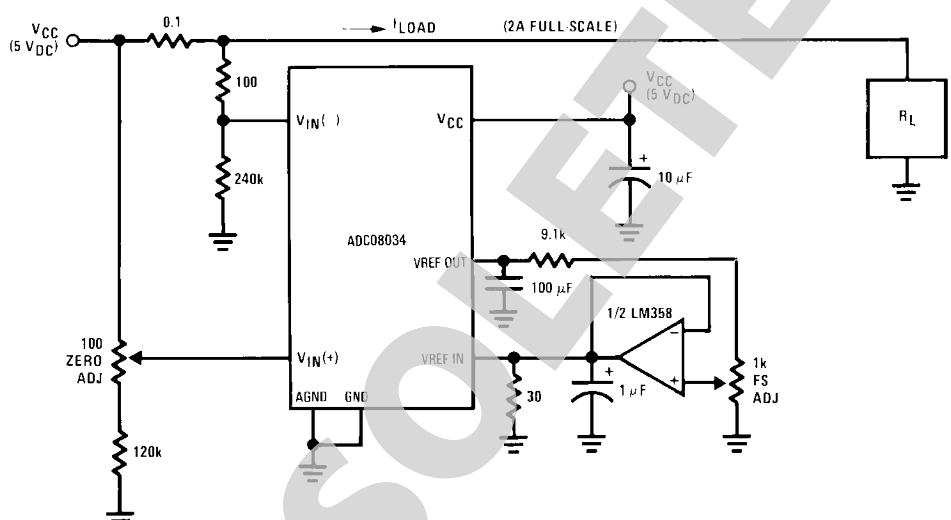
10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Low-Cost Remote Temperature Sensor



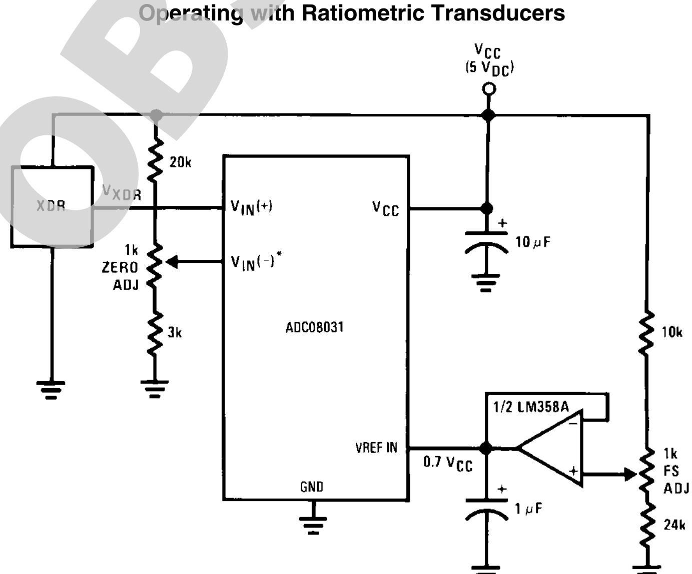
1055545

Digitizing a Current Flow



1055522

Operating with Ratiometric Transducers



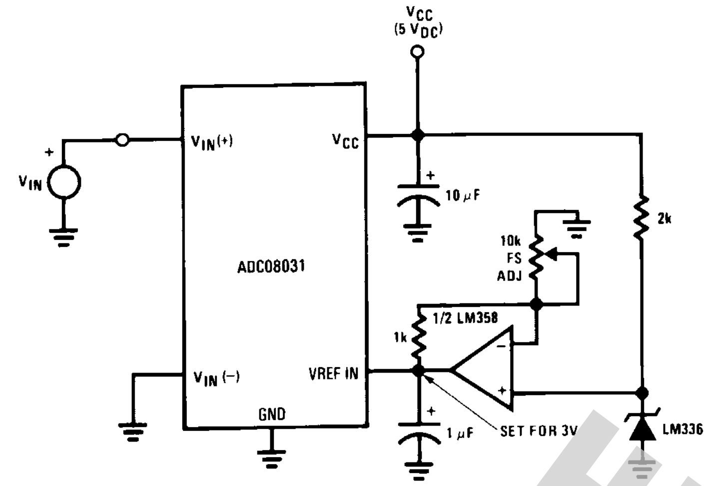
1055523

$^*V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \leq V_{XDR} \leq$ 85% of V_{CC}

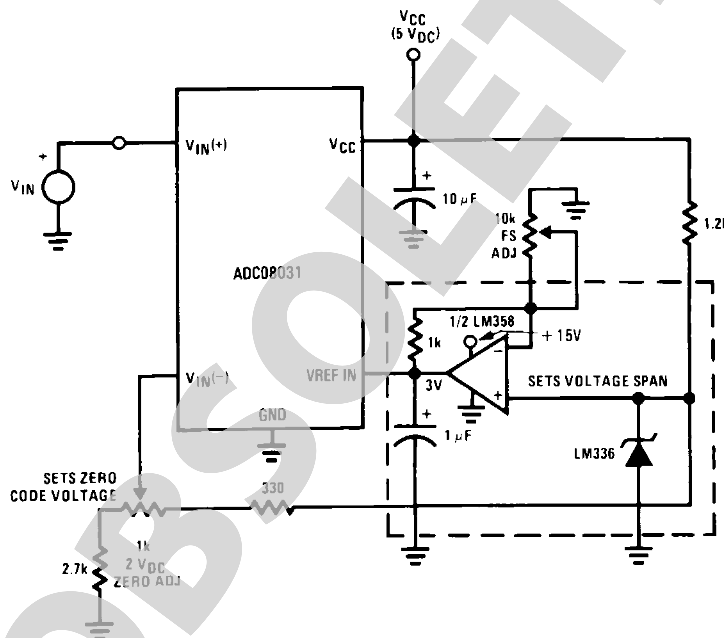
10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Span Adjust; 0V ≤ V_{IN} ≤ 3V



1055546

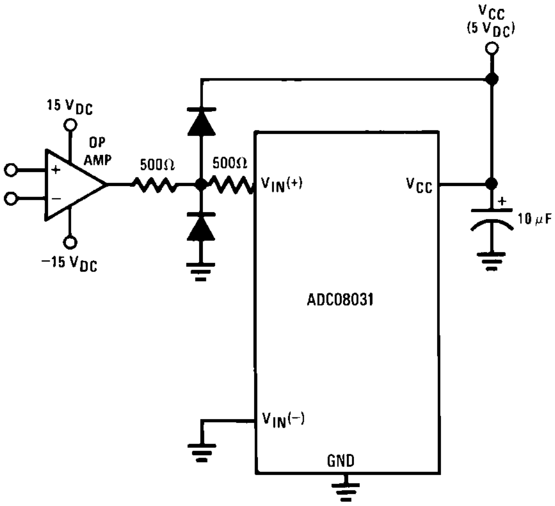
Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V



1055547

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

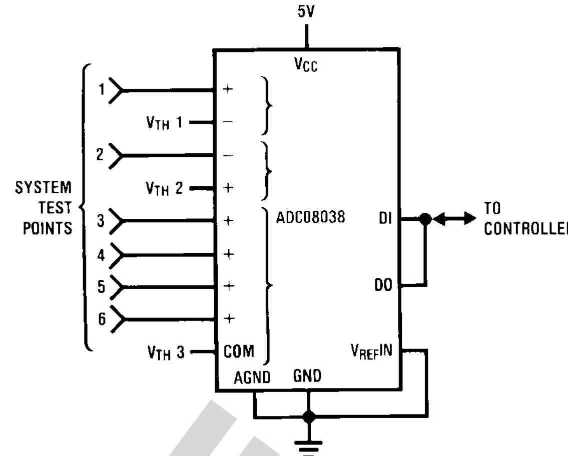
Protecting the Input



1055525

Diodes are 1N914

High Accuracy Comparators

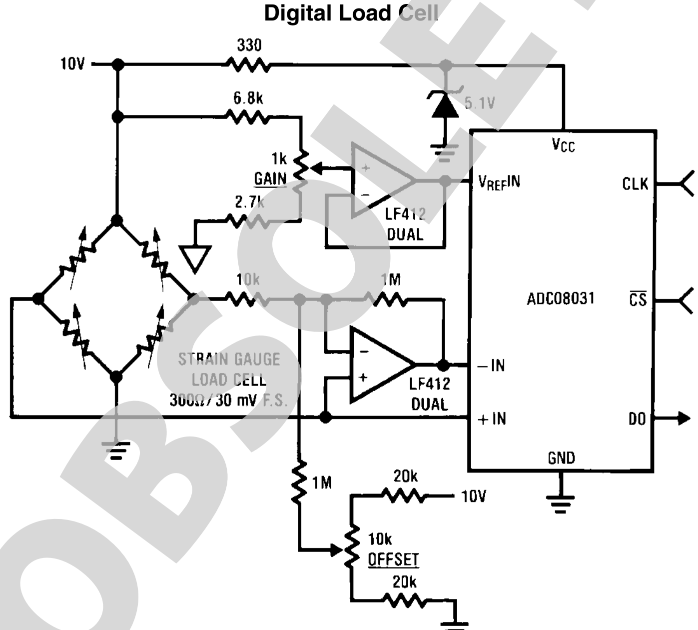


1055526

DO = all 1s if $+V_{IN} > -V_{IN}$

DO = all 0s if $+V_{IN} < -V_{IN}$

Digital Load Cell

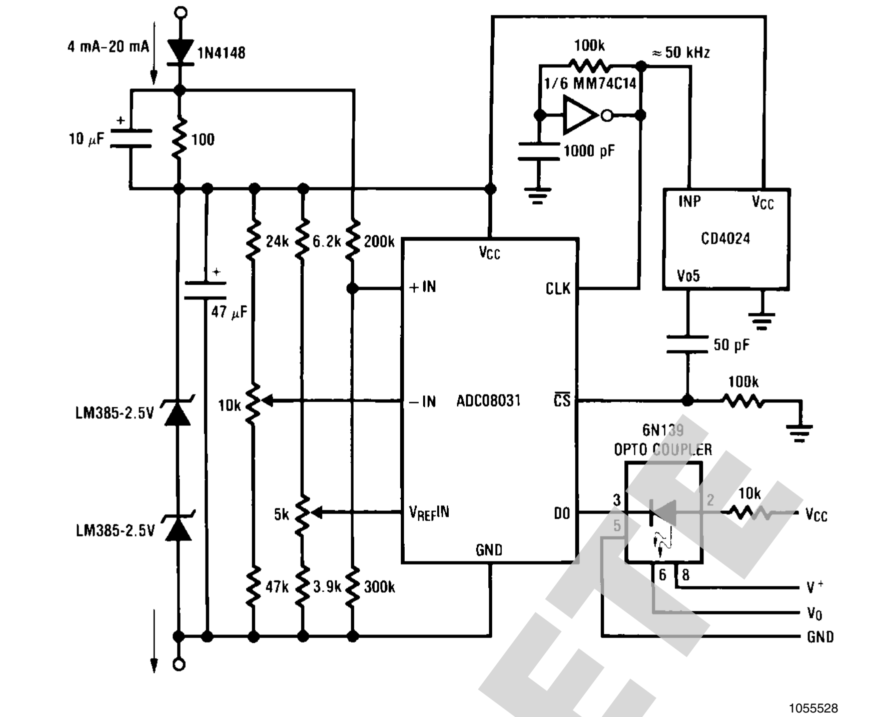


1055527

- Uses one more wire than load cell itself
- Two mini-DIPs could be mounted inside load cell for digital output transducer
- Electronic offset and gain trims relax mechanical specs for gauge factor and offset
- Low level cell output is converted immediately for high noise immunity

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

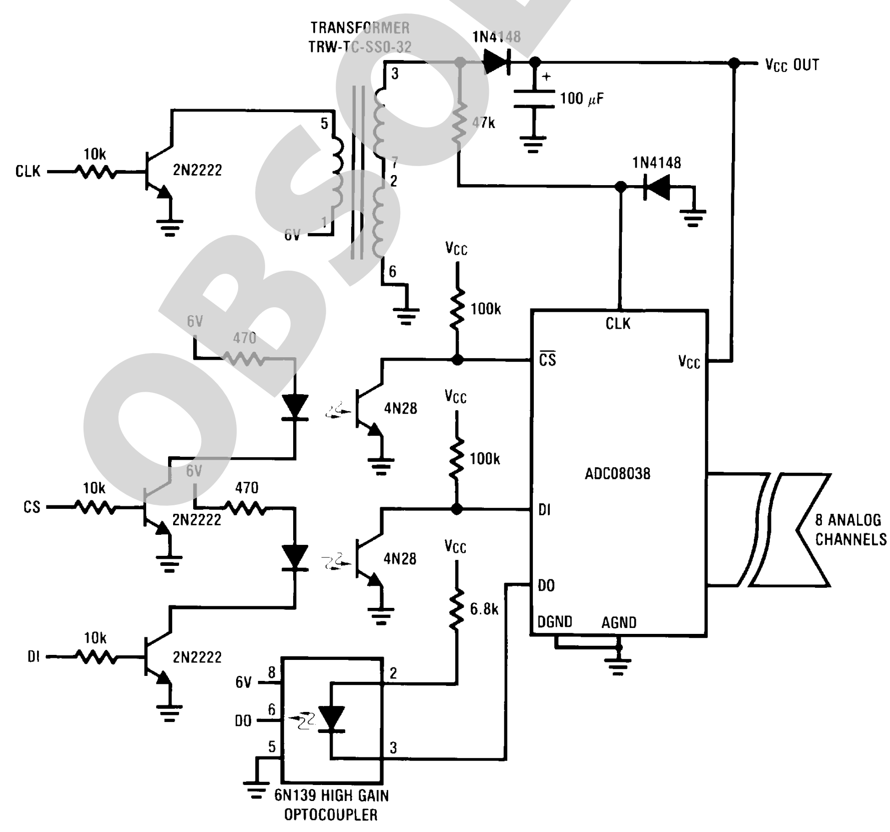
4 mA-20 mA Current Loop Converter



— All power supplied by loop

— 1500V isolation at output

Isolated Data Converter

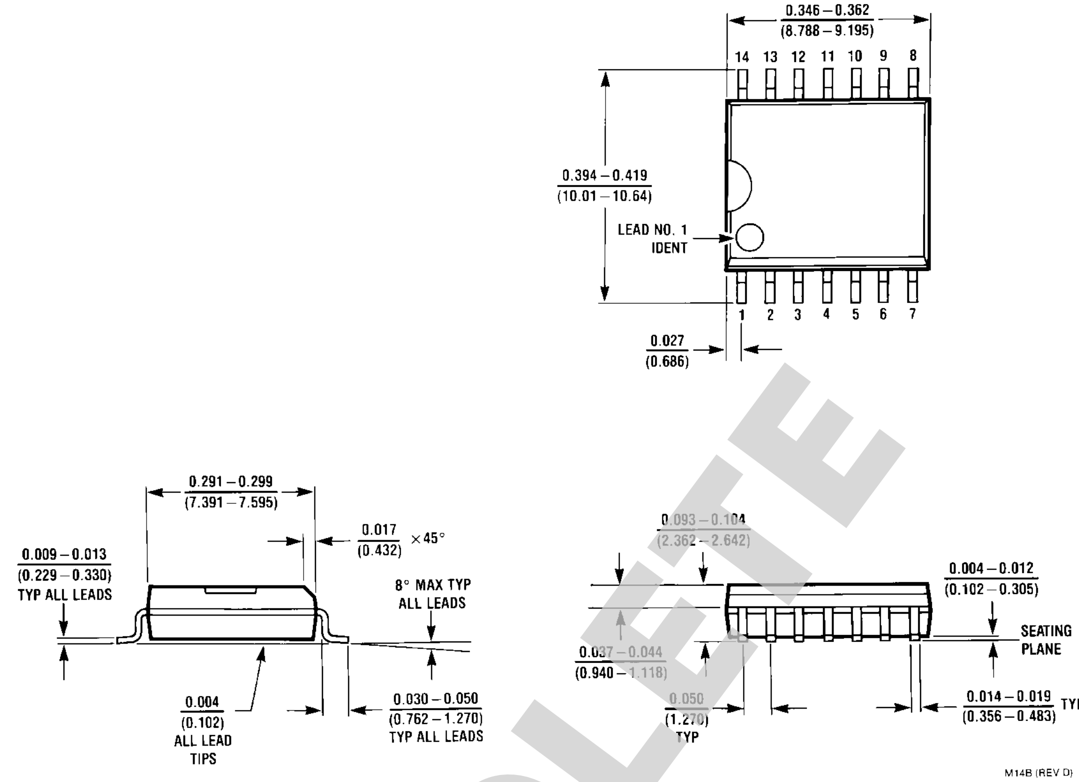


— No power required remotely

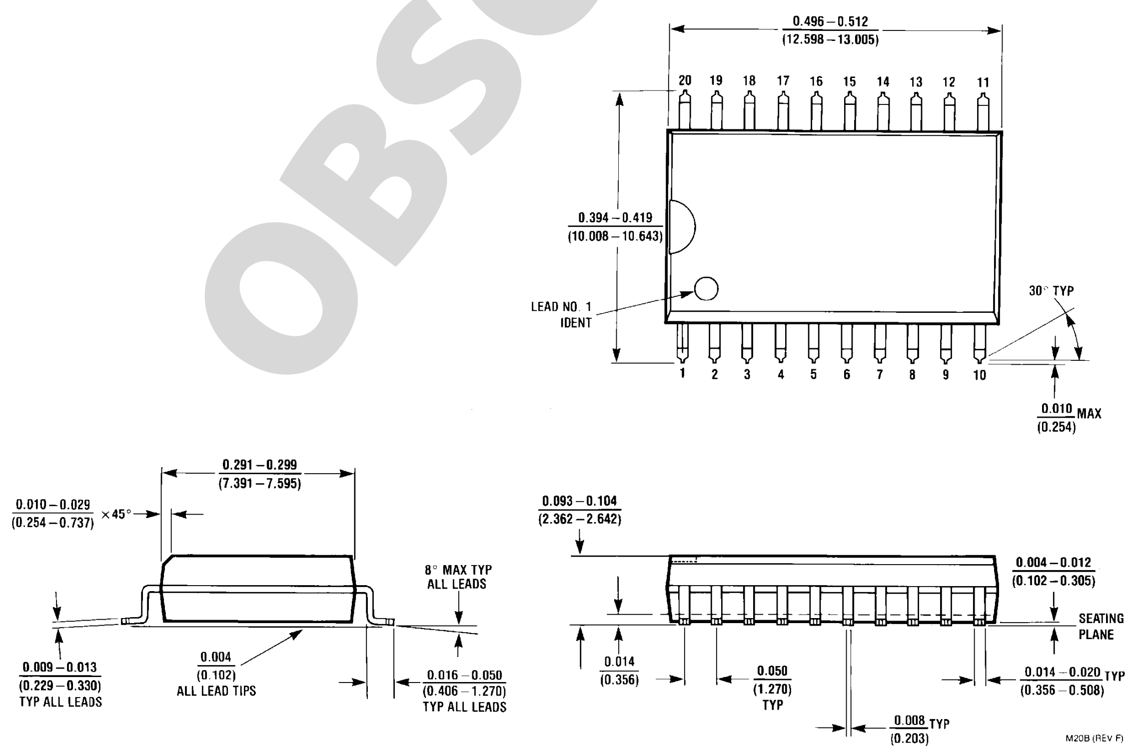
— 1500V isolation

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Physical Dimensions inches (millimeters) unless otherwise noted

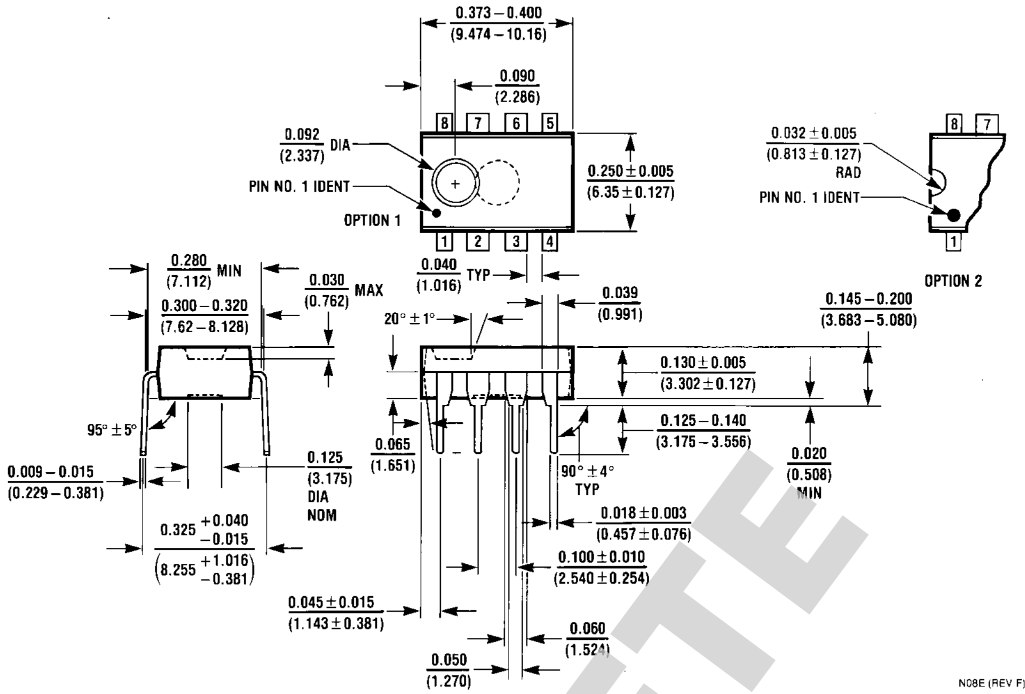


Order Number ADC08031CIWM, ADC08032CIWM, or ADC08034CIWM
NS Package Number M14B

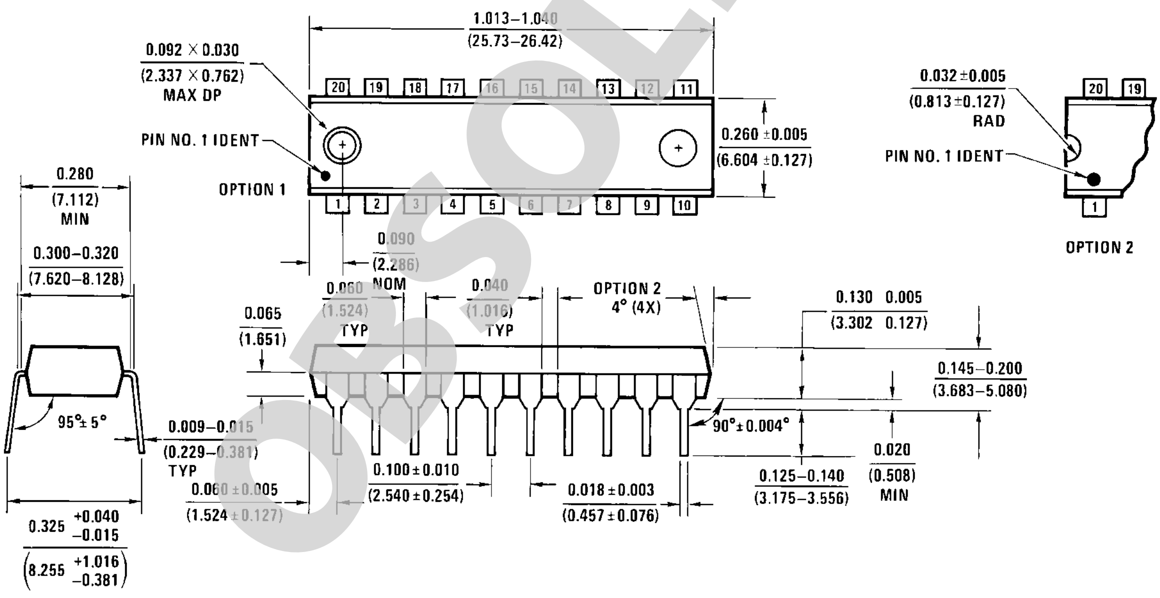


Order Number ADC08038CIWM
NS Package Number M20B

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10



Order Number ADC08031CIN
NS Package Number N08E



Order Number ADC08038CIN
NS Package Number N20A

10555 Version 6 Revision 6 Print Date/Time: 2008/01/10 20:18:10

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
Wireless (PLL/VCO)	www.national.com/wireless		

For the most current product information visit us at www.national.com

www.national.com

National Semiconductor Americas Technical Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
		TI E2E Community Home Page	e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265