Matched N-Channel JFET Pairs

PRODUCT SUMMARY					
Part Number	**$V_{GS(off)}$ (V)**	**$V_{(BR)GSS}$ Min (V)**	**g_{fs} Min (mS)**	**I_G Typ (pA)**	**$\|V_{GS1} - V_{GS2}\|$ Max (mV)**
U440	–1 to –6	–25	4.5	–1	10
U441	–1 to –6	–25	4.5	–1	20

FEATURES

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 85 dB.

BENEFITS

- Minimum Parasitics Ensuring Maximum High-Frequency Performance
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

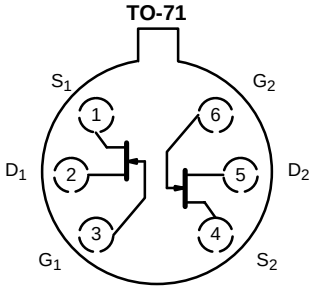
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

DESCRIPTION

The U440/441 are matched pairs of JFETs mounted in a single TO-71 package. This two-chip design reduces parasitics and gives better performance at very high frequencies while ensuring extremely tight matching. These devices are an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications.

The hermetically-sealed TO-71 package is available with full military screening per MIL-S-19500 (see Military Information).

For similar products in SO-8 packaging see the SST440/SST441 data sheet. For low-noise options, see the SST/U401 series data sheet. For low-leakage alternatives, see the U421/423 data sheet.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage . . . . . –25 V
Gate-Gate Voltage . . . . . ±50 V
Gate Current . . . . . 50 mA
Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300°C
Storage Temperature . . . . . –65 to 200°C

Operating Junction Temperature . . . . . –55 to 150°C
Power Dissipation : Per Side[a] . . . . . 250 mW
Total[b] . . . . . 500 mW

Notes
a. Derate 2 mW/°C above 25°C
b. Derate 4 mW/°C above 25°C

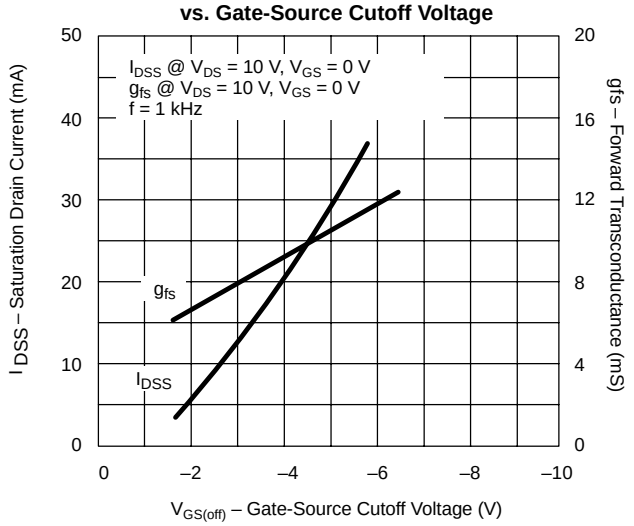
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Typ[a]	Limits U440 Min	Limits U440 Max	Limits U441 Min	Limits U441 Max	Unit
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 μA, V_{DS} = 0 V	–35	–25		–25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 nA	–3.5	–1	–6	–1	–6	V
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = –15 V, V_{DS} = 0 V	–1		–500		–500	pA
		T_A = 125°C	–2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	–1		–500		–500	pA
		T_A = 125°C	–0.3					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA , V_{DS} = 0 V	0.7					V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 5 mA f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		70		200		200	μS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, I_D = 5 mA f = 1 MHz	3					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					pF
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DS} = 10 V, I_D = 5 mA f = 10 kHz	4					$nV/\sqrt{Hz}$
Matching								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	6		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA T_A = –55 to 125°C	20					μV/°C
Saturation Drain Current Ratio[c]	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.97					
Transconductance Ratio[c]	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 10 V, I_D = 5 mA f = 1 kHz	0.97					
Common Mode Rejection Ratio	CMRR	V_{DG} = 5 to 10 V, I_D = 5 mA	85					dB

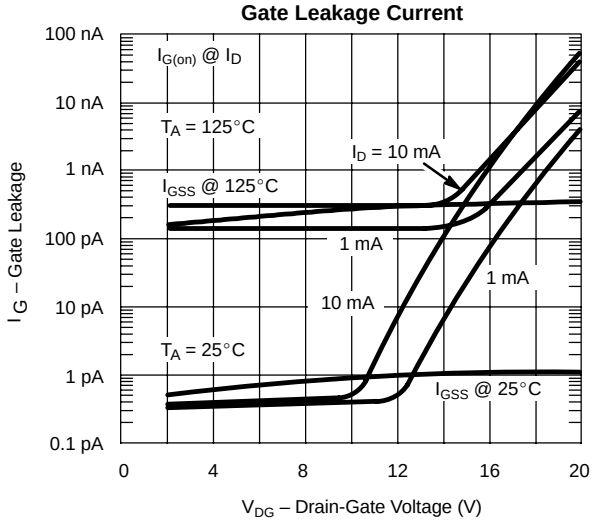
Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. NZFD
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
c. Assumes smaller value in the numerator.

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

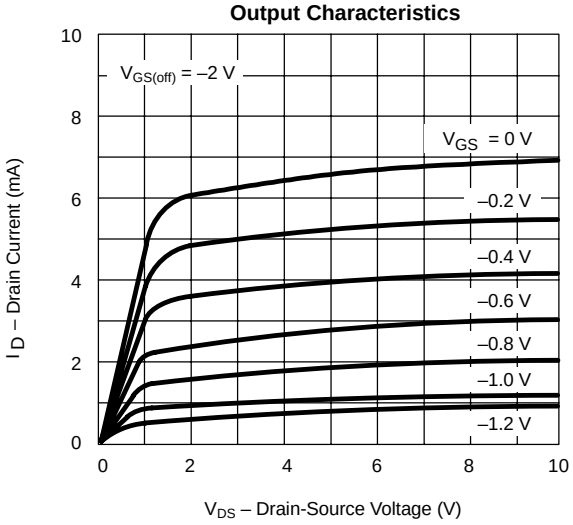
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



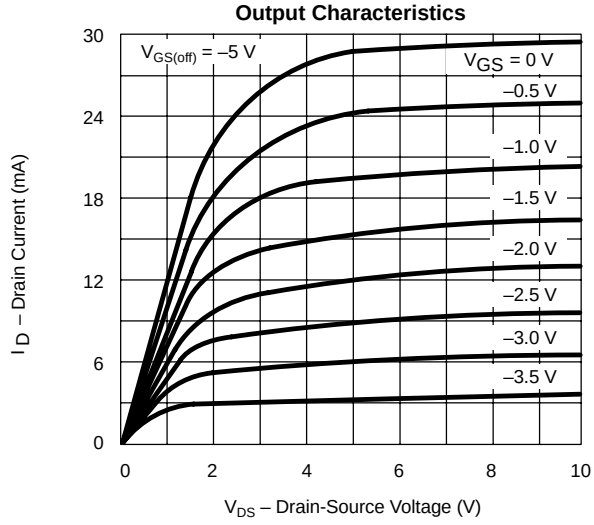
Gate Leakage Current



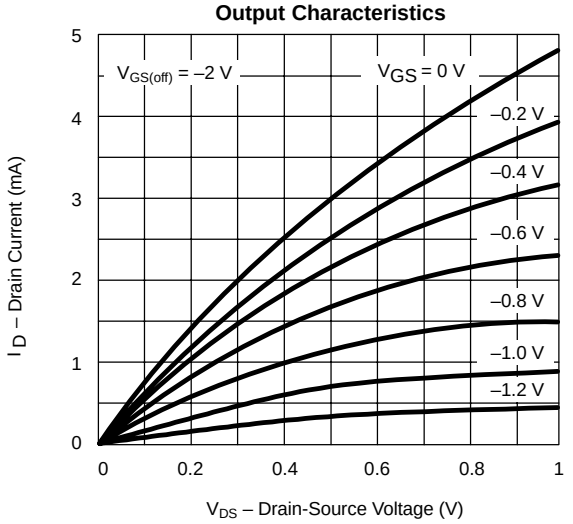
Output Characteristics



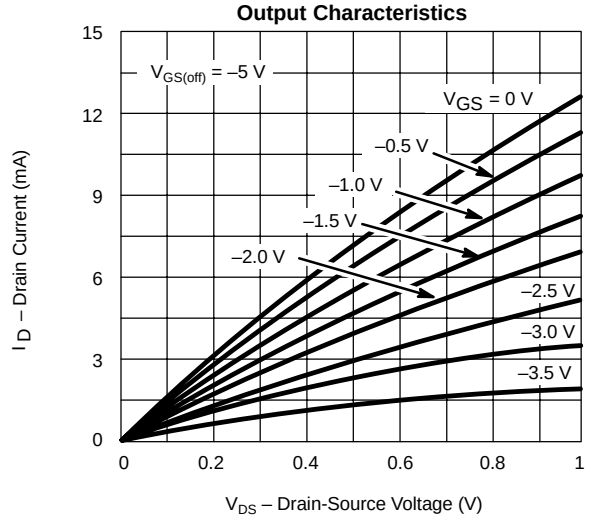
Output Characteristics



Output Characteristics

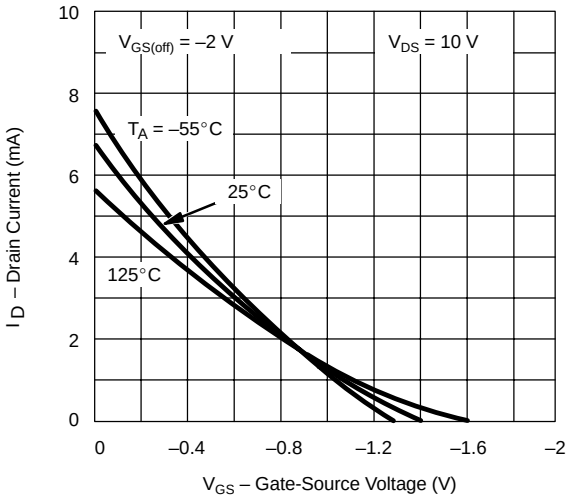


Output Characteristics

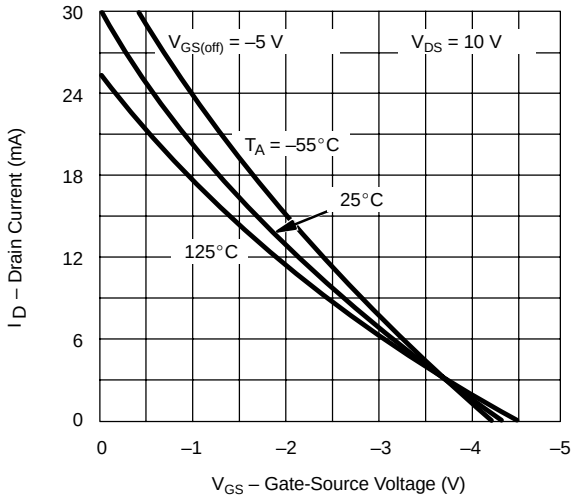


TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

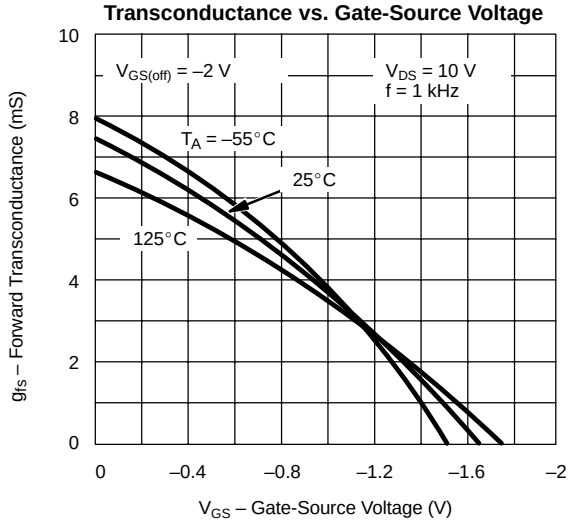
Transfer Characteristics



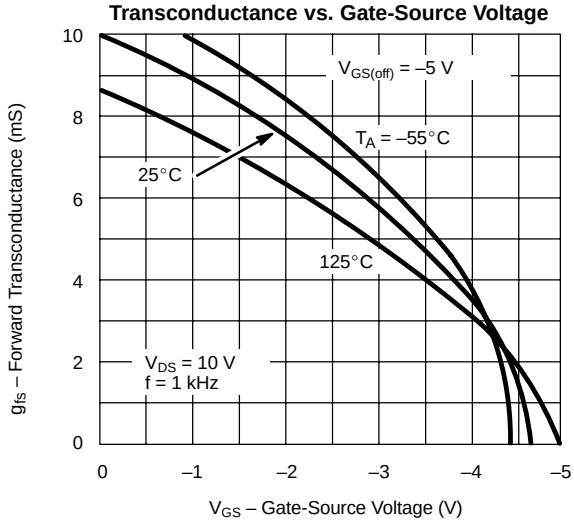
Transfer Characteristics



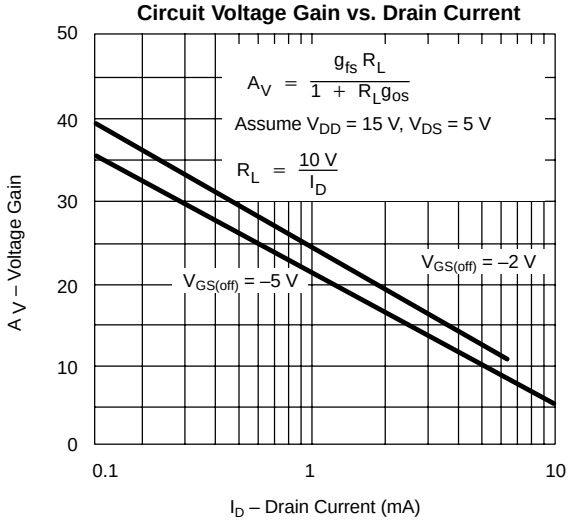
Transconductance vs. Gate-Source Voltage



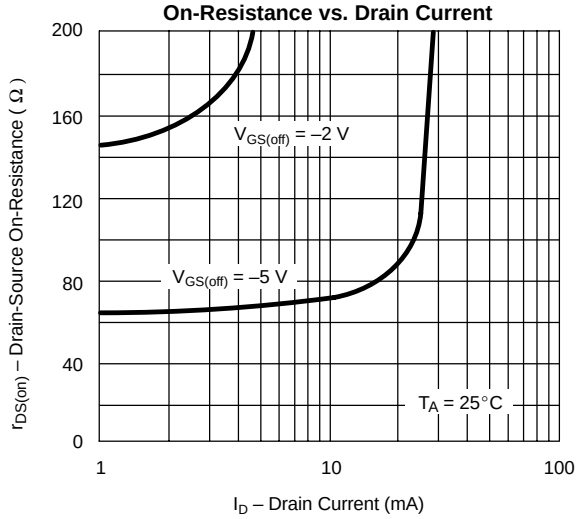
Transconductance vs. Gate-Source Voltage



Circuit Voltage Gain vs. Drain Current



On-Resistance vs. Drain Current



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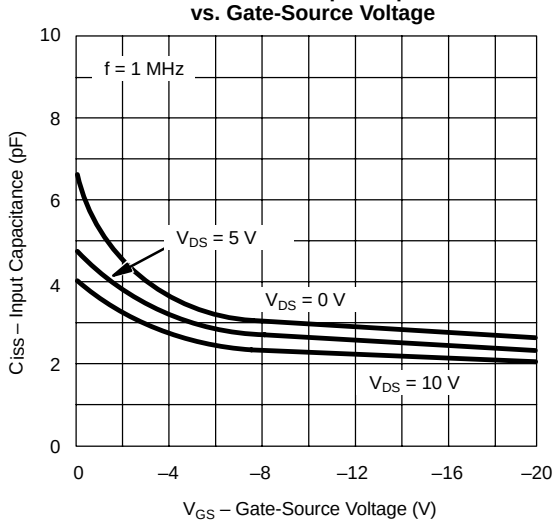
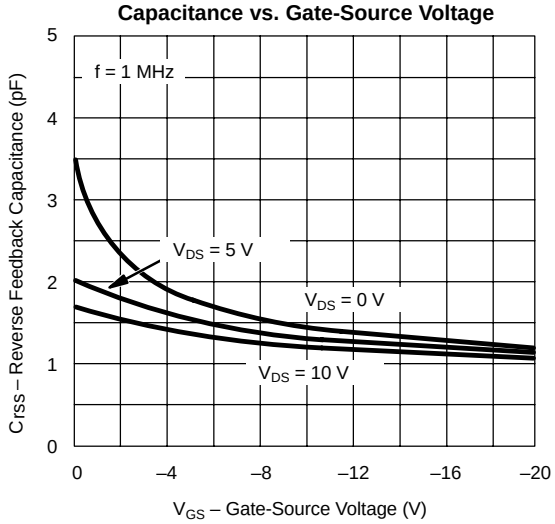
TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

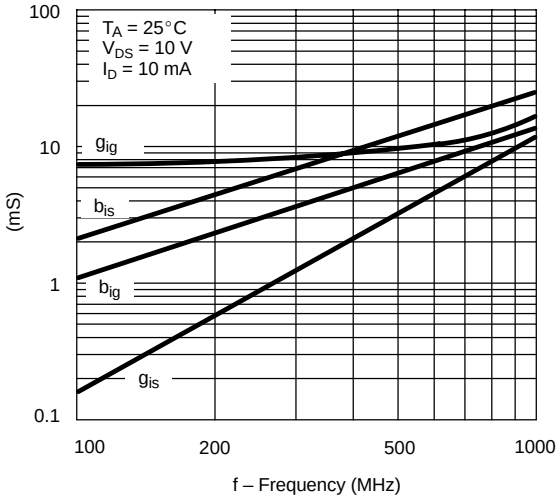
Common-Source Input Capacitance vs. Gate-Source Voltage



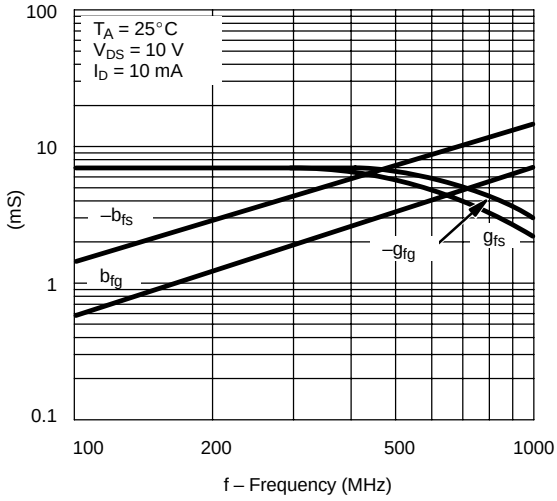
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



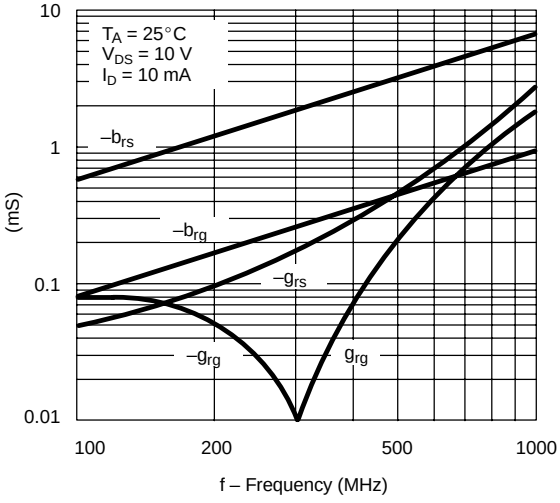
Input Admittance



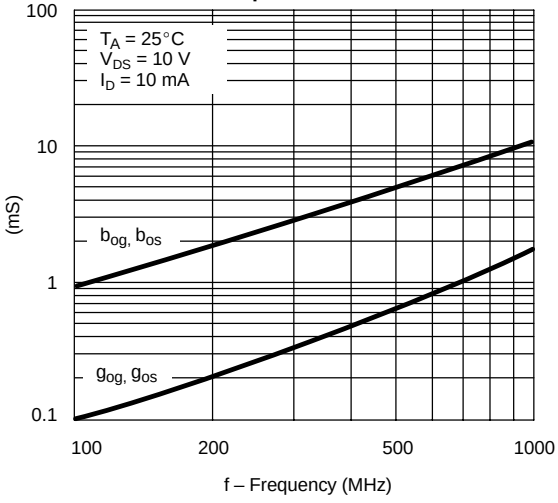
Forward Admittance



Reverse Admittance



Output Admittance



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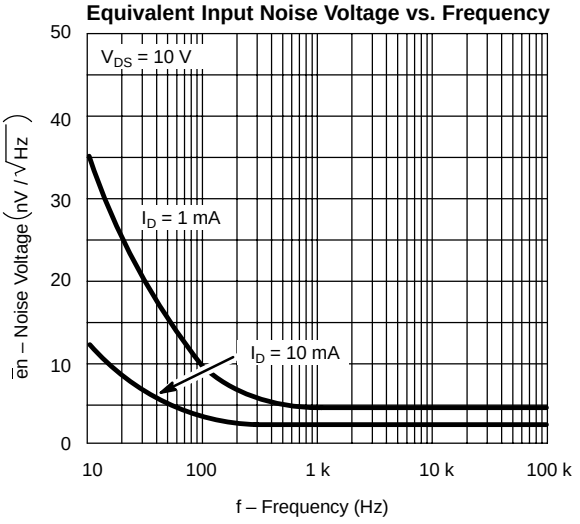
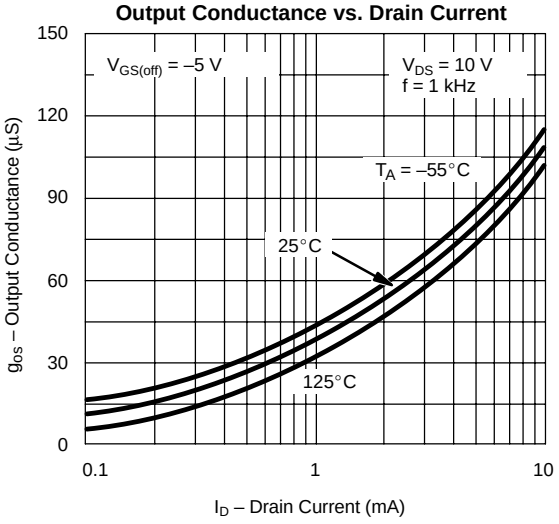
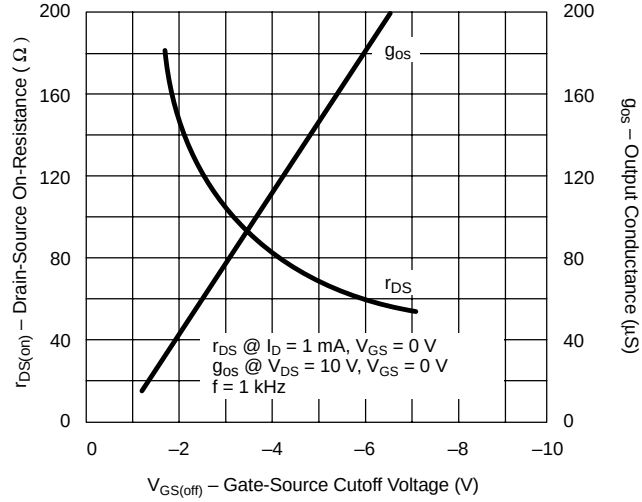
Equivalent Input Noise Voltage vs. Frequency



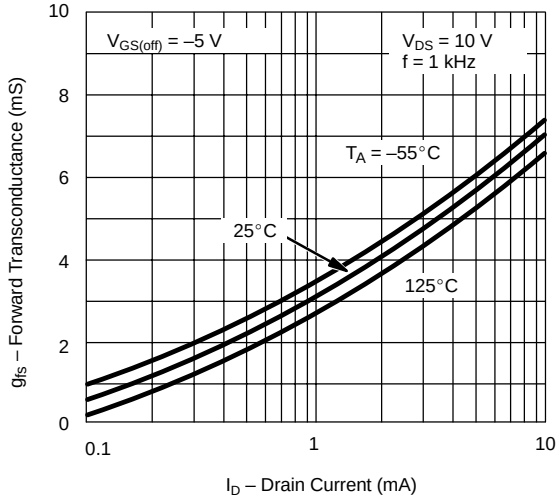
Output Conductance vs. Drain Current



On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage



Common-Source Forward Transconductance vs. Drain Current



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