

Vishay Siliconix

COMPLIANT

# N-Channel 150-V (D-S) 175 °C MOSFET

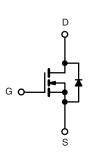
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)		
150	0.052 at V <sub>GS</sub> = 10 V	25		
150	0.060 at V <sub>GS</sub> = 6 V	23		



- TrenchFET<sup>®</sup> Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized
- 100 % Rg Tested
- Compliant to RoHS Directive 2002/95/EC

#### **APPLICATIONS**

• Primary Side Switch



N-Channel MOSFET

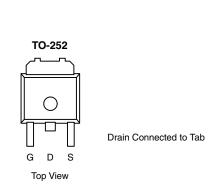
<b>ABSOLUTE MAXIMUM RATINGS</b> $T_A = 25 \text{ °C}$ , unless otherwise noted						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage	V <sub>DS</sub>	150	Ň			
Gate-Source Voltage	V <sub>GS</sub>	± 20	V			
Continuous Drain Current (T 175 °C)b	T <sub>C</sub> = 25 °C	L	25			
Continuous Drain Current (T <sub>J</sub> = 175 °C) <sup>b</sup>	T <sub>C</sub> = 125 °C	I <sub>D</sub>	14.5			
Pulsed Drain Current	I <sub>DM</sub>	50	А			
Continuous Source Current (Diode Conduction)	۱ <sub>S</sub>	25				
Avalanche Current	I <sub>AR</sub>	25				
Repetitive Avalanche Energy (Duty Cycle $\leq$ 1 %)	L = 0.1 mH	E <sub>AR</sub>	31	mJ		
	T <sub>C</sub> = 25 °C	P <sub>D</sub>	136 <sup>b</sup>	w		
Maximum Power Dissipation	T <sub>A</sub> = 25 °C		3 <sup>a</sup>	vv		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
lunation to Amhionta	t ≤ 10 s	R <sub>thJA</sub>	15	18	°C/W		
Junction-to-Ambient <sup>a</sup>	Steady State		40	50			
Junction-to-Case (Drain)		R <sub>thJC</sub>	0.85	1.1			

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See SOA curve for voltage derating.



Ordering Information:

SUD25N15-52-E3 (Lead (Pb)- free)

## SUD25N15-52

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Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static		· · · · · · · · · · · · · · · · · · ·					
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS}$ = 0 V, I <sub>D</sub> = 250 µA	150			v	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2		4	v	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ = 150 V, $V_{GS}$ = 0 V, $T_{J}$ = 125 °C			50	μΑ	
		$V_{DS} = 150 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 175 ^{\circ}\text{C}$			250		
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 V, V_{GS} = 10 V$	50			А	
		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	0.042 0		0.052		
- · · · · · · · · · · · · · · · · · · ·	P	$V_{GS}$ = 10 V, $I_{D}$ = 5 A, $T_{J}$ = 125 °C			0.109	1	
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	$V_{GS}$ = 10 V, I <sub>D</sub> = 5 A, T <sub>J</sub> = 175 °C			0.145	Ω	
		$V_{GS} = 6 V, I_D = 5 A$		0.047	0.060		
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A		40		S	
Dynamic <sup>a</sup>							
Input Capacitance	C <sub>iss</sub>			1725			
Output Capacitance	C <sub>oss</sub>	$V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz		216		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			100			
Total Gate Charge <sup>c</sup>	Qg			33	40		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 75 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 25 \text{ A}$		9		nC	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			12		1	
Gate Resistance	Rg		1		3	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			15	25		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, \text{ R}_{L} = 3 \Omega$		70	100	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$\text{I}_\text{D} \cong$ 25 A, $\text{V}_\text{GEN}$ = 10 V, $\text{R}_\text{g}$ = 2.5 $\Omega$		25	40		
Fall Time <sup>c</sup>	t <sub>f</sub>			60	90		
Source-Drain Diode Ratings and Cha	racteristics	Γ <sub>C</sub> = 25 °C			I		
Pulsed Current	I <sub>SM</sub>				50	А	
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_{F} = 25 \text{ A}, V_{GS} = 0 \text{ V}$		0.9	1.5	V	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 25 A, dl/dt = 100 A/μs		95	140	ns	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

c. Independent of operating temperature.

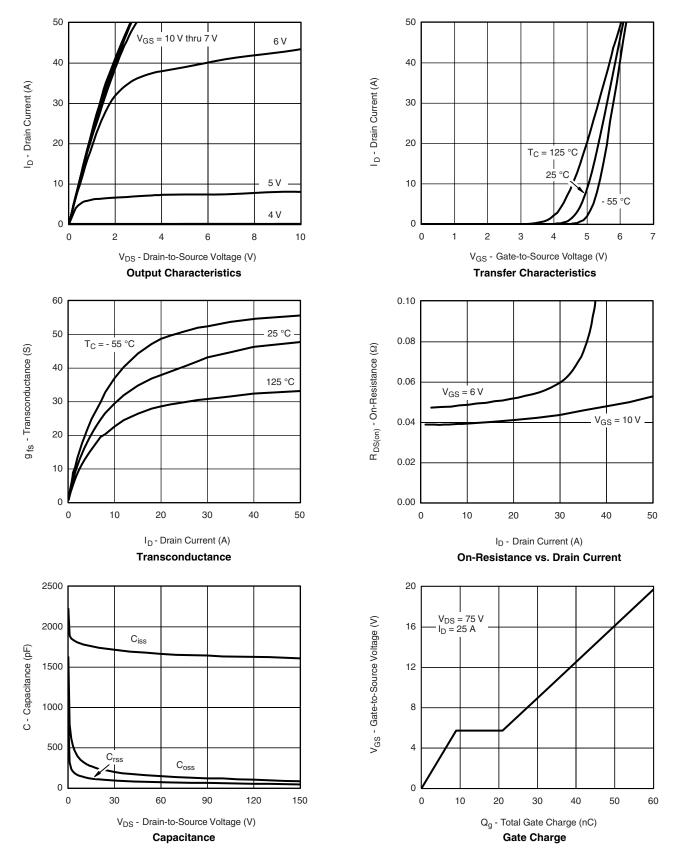
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



# SUD25N15-52

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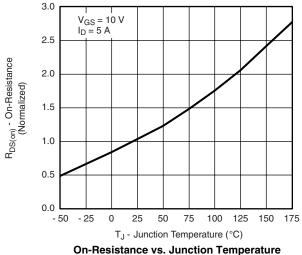
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



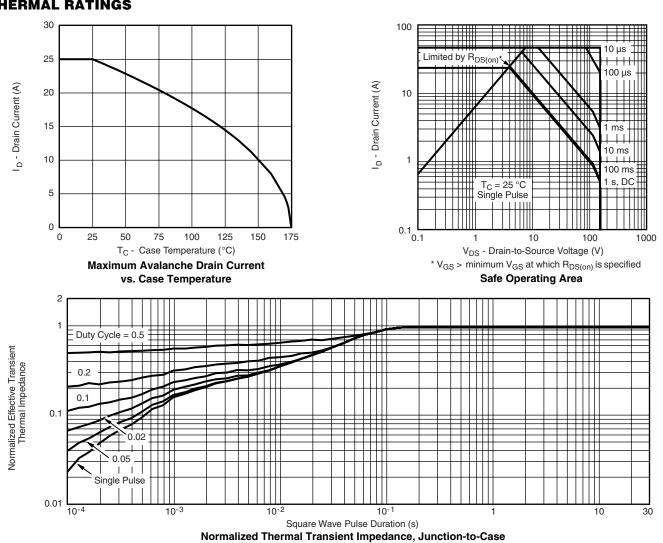
Document Number: 71768 S09-1501-Rev. D, 10-Aug-09

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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







100

10

1

0

0.3

T<sub>J</sub> = 150 °C

0.6

V<sub>SD</sub> - Source-to-Drain Voltage (V)

Source-Drain Diode Forward Voltage

I<sub>S</sub> - Source Current (A)

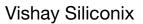
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71768.



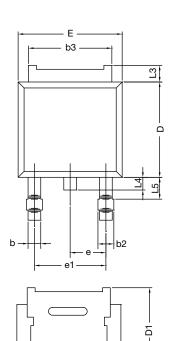
T<sub>J</sub> = 25 °C

0.9

1.2







E1

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**TO-252AA** Case Outline

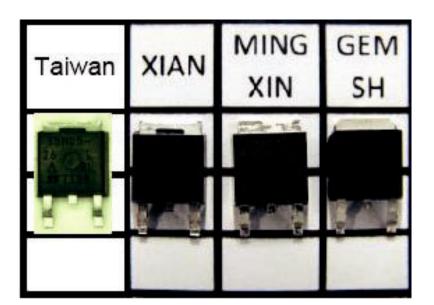
	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
А	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
E	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28	BSC	0.090 BSC		
e1	4.56	4.56 BSC		BSC	
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T13- DWG: 534	0359-Rev. O, 7	03-Jun-13			

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Notes

• Dimension L3 is for reference only.

• Xi'an, Mingxin, and GEM SH actual photo.



Revision: 03-Jun-13

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#### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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