SWITCHMODE [™] Series NPN Silicon Power Transistor

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ $T_C = 100$ °C
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C
 t_C @ 1 A, 100°C is 290 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CEO(sus)}	400	Vdc
Collector–Emitter Voltage	VCEV	700	Vdc
Emitter Base Voltage	VEBO	9	Vdc
Collector Current - Continuous - Peak (Note 1.)	I _{CM}	1.5 3	Adc
Base Current - Continuous - Peak (Note 1.)	I _B	0.75 1.5	Adc
Emitter Current – Continuous – Peak (Note 1.)	I _E	2.25 4.5	Adc
Total Power Dissipation @ T _A = 25°C Derate above 25°C	PD	1.4 11.2	Watts mW/°C
Total Power Dissipation @ T _C = 25°C Derate above 25°C	PD	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction to Ambient	$R_{ heta JA}$	89	°C/W
Maximum Load Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	TL	275	°C

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



http://onsemi.com

1.5 AMPERES
NPN SILICON POWER
TRANSISTORS
300 AND 400 VOLTS
40 WATTS



TO-225 CASE 77 STYLE 3

MARKING DIAGRAM



Y = Year WW = Work Week MJE13003 = Device Code

ORDERING INFORMATION

Device	Package	Shipping		
MJE13003	TO-225	500 Units/Box		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS	6 (Note 2.)					
Collector–Emitter Sustai (I _C = 10 mA, I _B = 0)	VCEO(sus)	400	_	-	Vdc	
Collector Cutoff Current (V _{CEV} = Rated Value (V _{CEV} = Rated Value	ICEV	- -	_ _	1 5	mAdc	
Emitter Cutoff Current (V _{EB} = 9 Vdc, I _C = 0)		IEBO	_	-	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Coll	ector Current with bass forward biased	I _{S/b}	Ç	See Figure 1	1	
Clamped Inductive SOA	with base reverse biased	RBSOA	5	See Figure 1	2	
ON CHARACTERISTICS	(Note 2.)					
DC Current Gain (IC = 0.5 Adc, VCE = 2) (IC = 1 Adc, VCE = 2)		hFE	8 5	_ _	40 25	_
Collector–Emitter Satura ($IC = 0.5$ Adc, $IB = 0.1$ ($IC = 1$ Adc, $IB = 0.25$ ($IC = 1.5$ Adc, $IB = 0.5$ ($IC = 1$ Adc, $IB = 0.25$	VCE(sat)	- - -		0.5 1 3 1	Vdc	
Base–Emitter Saturation (I _C = 0.5 Adc, I _B = 0.1 (I _C = 1 Adc, I _B = 0.25 (I _C = 1 Adc, I _B = 0.25	VBE(sat)	- - -	- - -	1 1.2 1.1	Vdc	
DYNAMIC CHARACTERI	STICS				<u>I</u>	
Current–Gain – Bandwid (I _C = 100 mAdc, V _{CE}		fT	4	10	_	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0), f = 0.1 MHz)	C _{ob}	-	21	_	pF
SWITCHING CHARACTE	RISTICS					1
Resistive Load (Table 1	1)					
Delay Time		t _d	_	0.05	0.1	μs
Rise Time	(V _{CC} = 125 Vdc, I _C = 1 A,	t _r	_	0.5	1	μs
Storage Time	- I _{B1} = I _{B2} = 0.2 A, t _p = 25 μs, Duty Cycle ≤ 1%)	t _S	_	2	4	μs
Fall Time	1 1, 2, 2, 2, 2, 2, 2, 3, 4	t _f	_	0.4	0.7	μs
Inductive Load, Clamp	ed (Table 1, Figure 13)	<u> </u>		1	l	<u> </u>
Storage Time		t _{sv}	_	1.7	4	μs
Crossover Time	(I _C = 1 A, V _{clamp} = 300 Vdc,	t _C	_	0.29	0.75	μs
Fall Time	$I_{B1} = 0.2 \text{ A}, V_{BE(off)} = 5 \text{ Vdc}, T_{C} = 100^{\circ}\text{C})$	t _{fi}		0.15	_	μs
		111			l	μ-0

^{2.} Pulse Test: PW = 300 μ s, Duty Cycle \leq 2%.

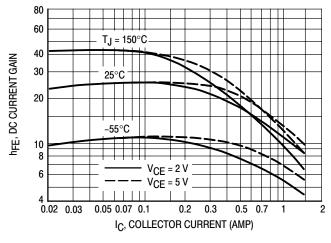


Figure 1. DC Current Gain

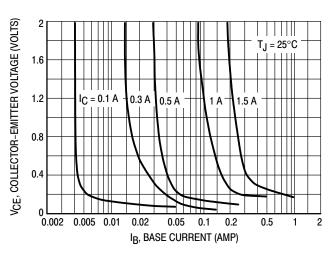


Figure 2. Collector Saturation Region

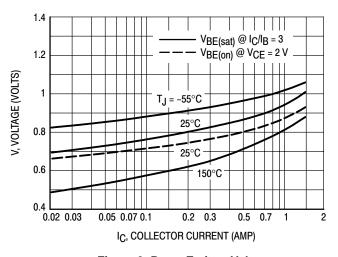


Figure 3. Base-Emitter Voltage

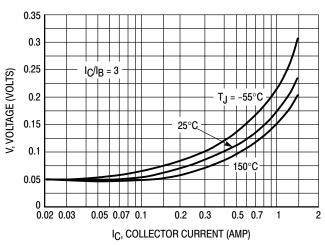


Figure 4. Collector-Emitter Saturation Region

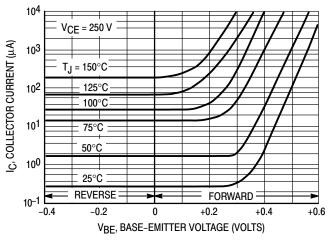


Figure 5. Collector Cutoff Region

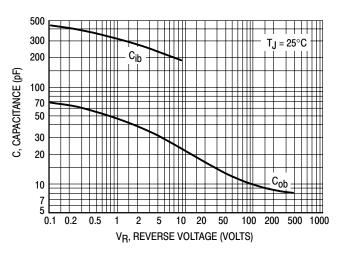


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	DUTY CYCLE \leq 10% $_{1N4933}$ \geq $_{1N4933}$ $>$ $_{1N4933}$	+125 V RC TUT SCOPE -4.0 V
CIRCUIT	Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20 GAP for 30 mH/2 A L _{Coil} = 50 mH V _{CC} = 20 V V _{clamp} = 300 Vdc	V_{CC} = 125 V R_{C} = 125 Ω D1 = 1N5820 or Equiv. R_{B} = 47 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS $t_{f} \text{ CLAMPED} \\ t_{f} \text{ CLAMPED} \\ t_{f} \Rightarrow \frac{t_{f} \text{ Clampent}}{V_{Clamp}}$ $t_{f} \approx \frac{L_{coil} (C_{pk})}{V_{Clamp}}$	+10.3 V 25 μs t _r , t _f < 10 ns Duty Cycle = 1.0% R _B and R _C adjusted for desired I _B and I _C

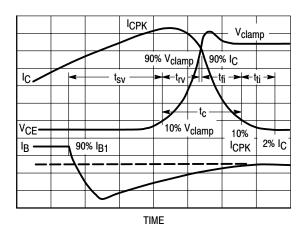


Table 2. Typical Inductive Switching Performance

I _C	T _C	t _{sv}	t _{rv}	t _{fi}	t _{ti}	t _C
	°C	μs	μs	μ s	μs	μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

Figure 7. Inductive Switching Measurements

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

 t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

tti = Current Tail, 10-2% IC

 t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

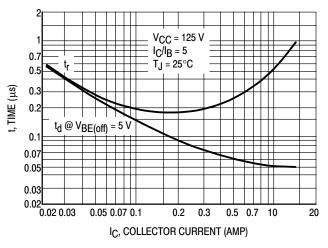
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

 $PSWT = 1/2 VCCIC(t_c)f$

In general, $t_{rV} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE



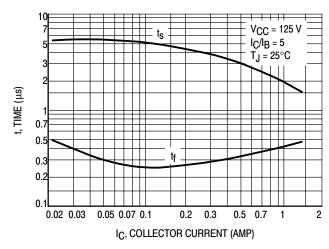


Figure 8. Turn-On Time

Figure 9. Turn-Off Time

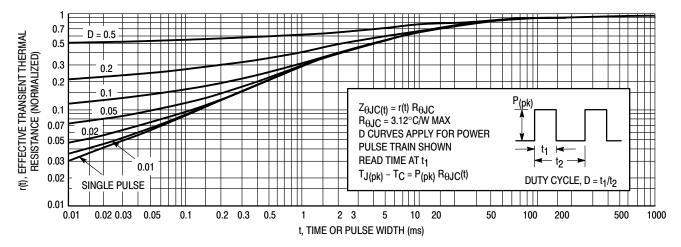


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

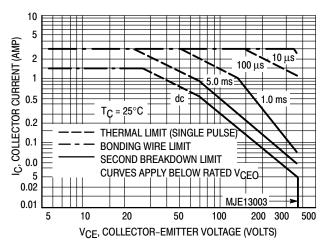


Figure 11. Active Region Safe Operating
Area

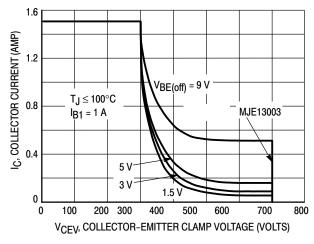


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25^{\circ}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

 $T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

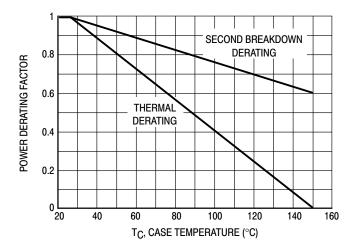
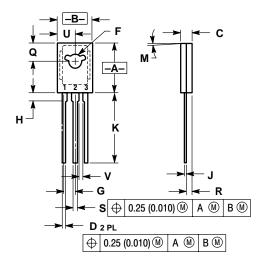


Figure 13. Forward Bias Power Derating

PACKAGE DIMENSIONS

TO-225 CASE 77-09 ISSUE W



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
 VIA EM 1082
- 2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.425	0.435	10.80	11.04	
В	0.295	0.305	7.50	7.74	
С	0.095	0.105	2.42	2.66	
D	0.020	0.026	0.51	0.66	
F	0.115	0.130	2.93	3.30	
G	0.094	BSC	2.39	BSC	
Н	0.050	0.095	1.27	2.41	
J	0.015	0.025	0.39	0.63	
K	0.575	0.655	14.61	16.63	
M	5°	ΓYP 5° TYP			
Q	0.148	0.158	3.76	4.01	
R	0.045	0.065	1.15	1.65	
S	0.025	0.035	0.64	0.88	
U	0.145	0.155	3.69	3.93	
٧	0.040		1.02		

STYLE 3: PIN 1. BASE

2. COLLECTOR 3. EMITTER

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