MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CE

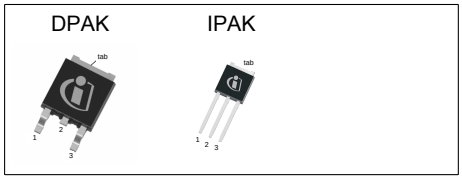
800V CoolMOS™ CE Power Transistor
IPx80R2K8CE

Data Sheet

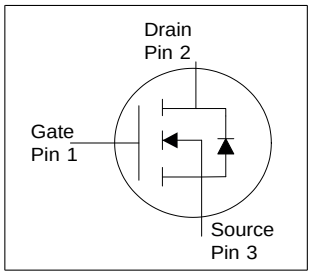
Rev. 2.2
Final

Power Management & Multimarket

1 Description



CoolMOS™ CE is a revolutionary technology for high voltage power MOSFETs. The high voltage capability combines safety with performance and ruggedness to allow stable designs at highest efficiency level. CoolMOS™ 800V CE comes with a selected package choice offering the benefit of reduced system costs and higher power density designs.



Features [1)]

- High voltage technology
- Extreme dv/dt rated
- High peak current capability
- Low gate charge
- Low effective capacitances
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- Pb-free lead plating; RoHS compliant; halogen free mold compound

Benefits

- Increased power density solutions due to smaller package
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to low operating temperatures

Applications

- LED Lighting for retrofit applications in QR Flyback topology

Table 1 Key Performance Parameters

Parameter	Value	Unit
T_{BQ} > R[illegible]	6..	T
P[illegible]	0,6	Ω
O[illegible]	/0	IA
G[illegible]	4	?
T[illegible]	1	T
A[illegible]	04	nD

Type / Ordering Code	Package	Marking	Related Links
GNB6.P0I6AC	NE+RM 030	6P0I6AC	qcc ?nncIbgv ?
GNS6.P0I6AC	NE+RM 03/		

Table of Contents

Bcqapgnrgml ,,,

2 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Amlrglsmsq bp_gl asppclr /'	I_D	+ +	+ +	/,7 /,/	?	T_C = 25ÁC T_C = 100ÁC
Nsjqcb bp_gl asppclr 0'	$I_{D,pulse}$	+	+	4	?	T_C=25ÁC
?t_j_lafc clcpew* qglejc nsjqc	E_{AS}	+	+	7.	kH	I_D =1A; V_{DD} = 50V
?t_j_lafc clcpew* pcncrgrgtc	E_{AR}	+	+	.,.3	kH	I_D =1A; V_{DD} = 50V
?t_j_lafc asppclr* pcncrgrgtc	I_{AR}	+	+	/	?	+
KMQDCR bt-br pseecblcqq	bt-br	+	+	3.	T-lq	V_{DS} =0...640V
E_rc qmspac tmjr_ec	V_{GS}	+0. +1.	+ +	0. 1.	T	qr_rga9 ?A &d</ Fx'
Nmucp bgqqgn_rgml &lml DsjjN? l ' RM+030* RM+03/	P_{tot}	+	+	20	U	T_C = 25ÁC
Mncp_rgle _lb qrmp_ec rcknep_rspc	T_j, T_{stg}	+33	+	/3.	ÄA	+
Amlrglsmsq bgmbc dmpu_pb asppclr	I_S	+	+	/,7	?	T_C = 25ÁC
Bgmbc nsjqc asppclr 0'	$I_{S,pulse}$	+	+	4	?	T_C = 25ÁC
Pctcpqc bgmbc bt-br 1'	bt-br	+	+	2	T-lq	V_{DS} =0...400V, I_{SD}≤I_S, T_j=25°C
K_vgksk bgmbc amk ksr_rgml qnccb	bg-br	+	+	2..	?-Éq	V_{DS} =0...400V, I_{SD}≤I_S, T_j=25°C

3 Thermal characteristics

Table 3 Thermal characteristics DPAK, IPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rfcpk_j pcqgqr_lac* hslargml +a_qc	R_{thJC}	+	+	1	ÄA-U	+
Rfcpk_j pcqgqr_lac* hslargml +_k`gclr 2'	R_{thJA}	+ +	+ 13	40 +	ÄA-U	QKB tcpqgml* bctgac ml NA@* kglgk_j dmmrnpglr QKB tcpqgml* bctgac ml NA@* 4ak 0 ammjgle _pc_ 2'
Qmjbcpgle rcknep_rspc* u_tc+ $ pcdjmuqmjbcpgle _jjmucb	T_{sold}	+	+	04.	ÄA	pcdjmu KQJ /

/' Jgkgrcb `w $R_{th\ k_v}$,

0' Nsjqc ugbrf r_n jgkgrcb `w $R_{th\ k_v}$

3) Identical low side and high side switch with identical R_G

2' Bctgac ml 2.kk(2.kk(/,3kk mlcj_wcp cnmvw NA@ DP2 ugrf 4ak 0 amnncp _pc_ &rfgailcqq 5.µk' dmp bp_gl amllcargml, NA@ gq tcprga_j ugrfmsr _gp qrpc_k ammjgle,

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Bp_gl+qmspac `pc_ibmul tmjr_ec	$V_{(BR)DSS}$	6..	+	+	T	V_{GS}=0V, I_D=0.25mA
E_rc rfpcqfmjb tmjr_ec	$V_{(GS)th}$	0,/	1	1,7	T	V_{DS}=V_{GS}, I_D=0.12mA
Xcpm e_rc tmjr_ec bp_gl asppclr	I_{DSS}	+ +	+ 03	3 +	É?	V_{DS}=800V, V_{GS}=0V, T_j=25°C V_{DS}=800V, V_{GS}=0V, T_j=150°C
E_rc+qmspac jc_i_ec aspclr	I_{GSS}	+	+	/..	l?	V_{GS}=20V, V_{DS}=0V
Bp_gl+qmspac ml+qr_rc pcqgqr_lac	$R_{DS(on)}$	+ +	0,2 4,3	0,6 +	Ω	V_{GS}=10V, I_D=1.1A, T_j=25°C V_{GS}=10V, I_D=1.1A, T_j=150°C
E_rc pcqgqr_lac	R_G	+	/,0	+	Ω	f=1 MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Glnsr a_n_agr_lac	C_{iss}	+	07.	+	nD	V_{GS}=0V, V_{DS}=100V, f=1MHz
Msrnsr a_n_agr_lac	C_{oss}	+	/1	+	nD	V_{GS}=0V, V_{DS}=100V, f=1MHz
Cddcargtc msrnsr a_n_agr_lac* clcpew pcj_rcb [1]	$C_{o(er)}$	+	//	+	nD	V_{GS}=0V, V_{DS}=0...480V
Cddcargtc msrnsr a_n_agr_lac* rgkc pcj_rcb [2]	$C_{o(tr)}$	+	04	+	nD	I_D=constant, V_{GS}=0V, V_{DS}=0...480V
Rspl+ml bcj_w rgkc	$t_{d(on)}$	+	03	+	lq	V_{DD}=400V, V_{GS}=0/10V, I_D=1.9A, R_G=47Ω
Pgqc rgkc	t_r	+	/3	+	lq	V_{DD}=400V, V_{GS}=0/10V, I_D=1.9A, R_G=47Ω
Rspl+mdd bcj_w rgkc	$t_{d(off)}$	+	50	+	lq	V_{DD}=400V, V_{GS}=0/10V, I_D=1.9A, R_G=47Ω
D_jj rgkc	t_f	+	/6	+	lq	V_{DD}=400V, V_{GS}=10 V, I_D=1.9A, R_G=47Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
E_rc rm qmspac af_pec	Q_{gs}	+	/,3	+	lA	V_{DD}=640V, I_D=1.9A, V_{GS}=0 to 10V
E_rc rm bp_gl af_pec	Q_{gd}	+	4	+	lA	V_{DD}=640V, I_D=1.9A, V_{GS}=0 to 10V
E_rc af_pec rmr_j	Q_g	+	/0	+	lA	V_{DD}=640V, I_D=1.9A, V_{GS}=0 to 10V
E_rc nj_rc_s tmjr_ec	$V_{plateau}$	+	3,3	+	T	V_{DD}=640V, I_D=1.9A, V_{GS}=0 to 10V

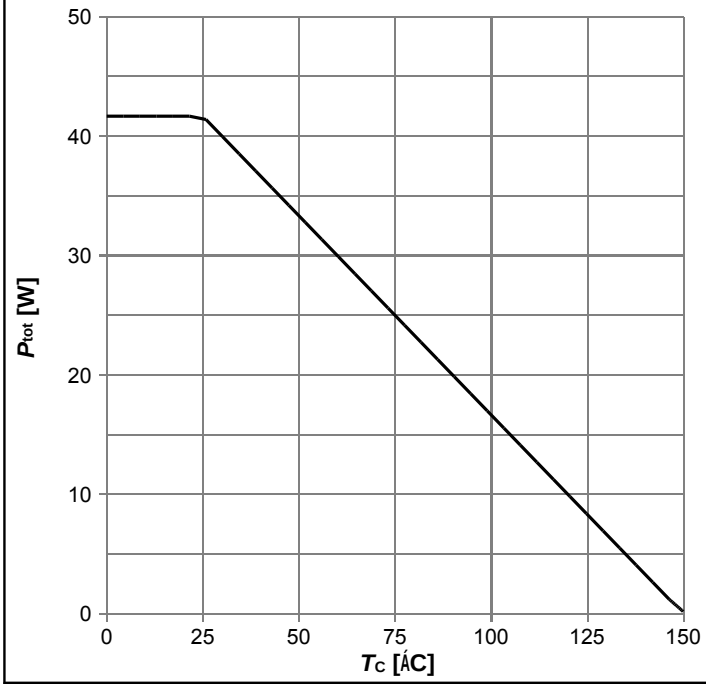
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Bgmbc dmpu_pb tmjr_ec	V_{SD}	+	/	/,0	T	V_{GS}=0V, I_F=1.9A, T_j=25°C
Pctcpqc pcamtcpw rgkc	t_{rr}	+	30.	+	lq	V_R=400V, I_F=1.9A, di_F/dt=100A/µs
Pctcpqc pcamtcpw af_pec	Q_{rr}	+	0	+	ÉA	V_R=400V, I_F=1.9A, di_F/dt=100A/µs
Nc_i pctcpqc pcamtcpw asppclr	I_{rrm}	+	4	+	?	V_R=400V, I_F=1.9A, di_F/dt=100A/µs

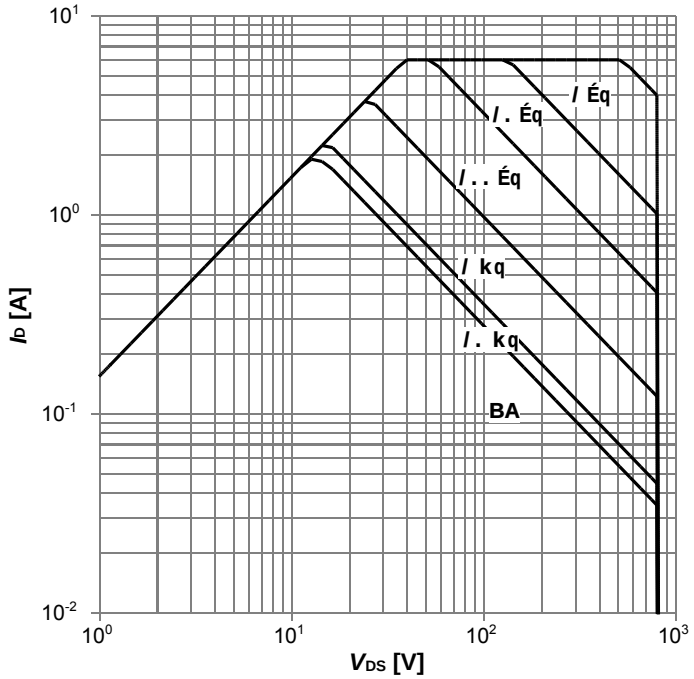
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



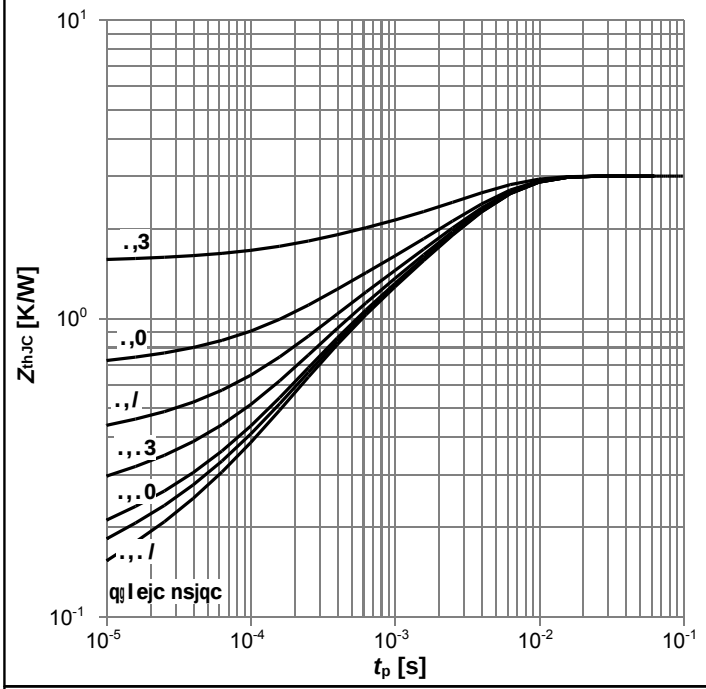
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



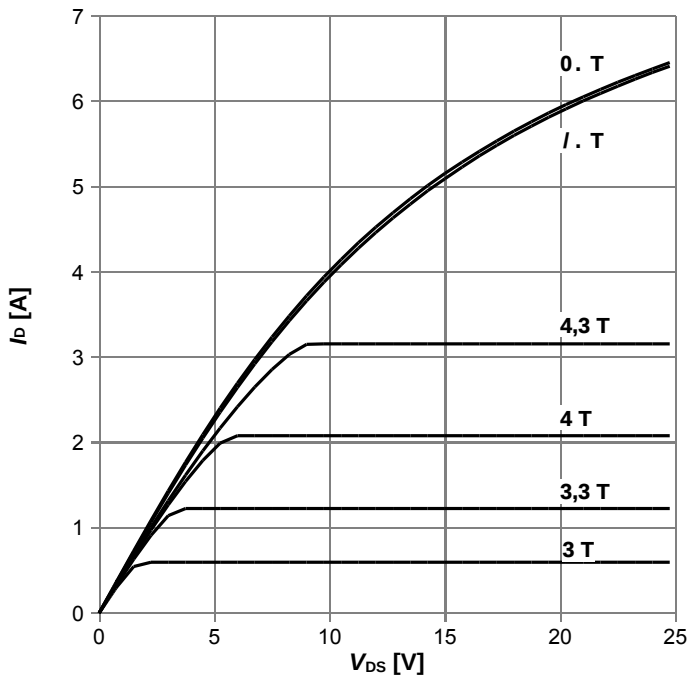
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 3: Max. transient thermal impedance



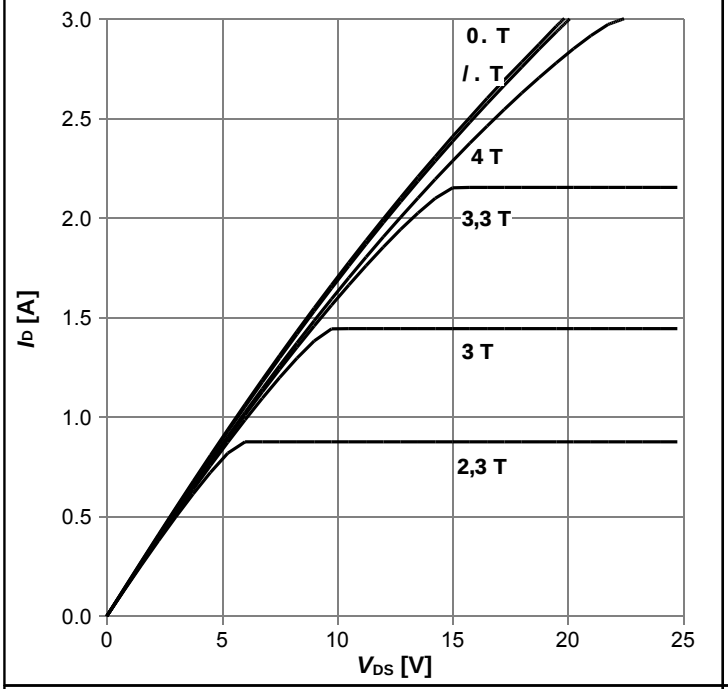
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 4: Typ. output characteristics



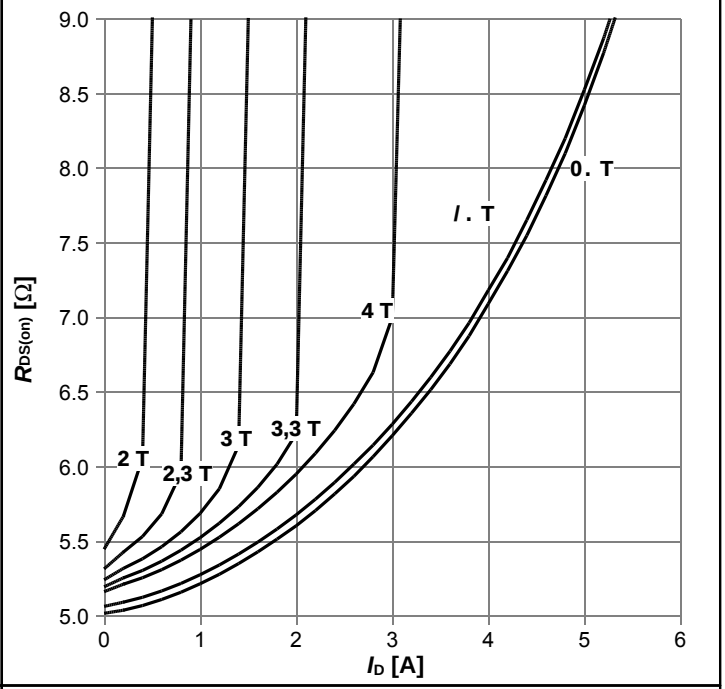
$I_D=f(V_{DS})$; T_j=25 °C; t_p=10 µs; parameter: V_{GS}

Diagram 5: Typ. output characteristics



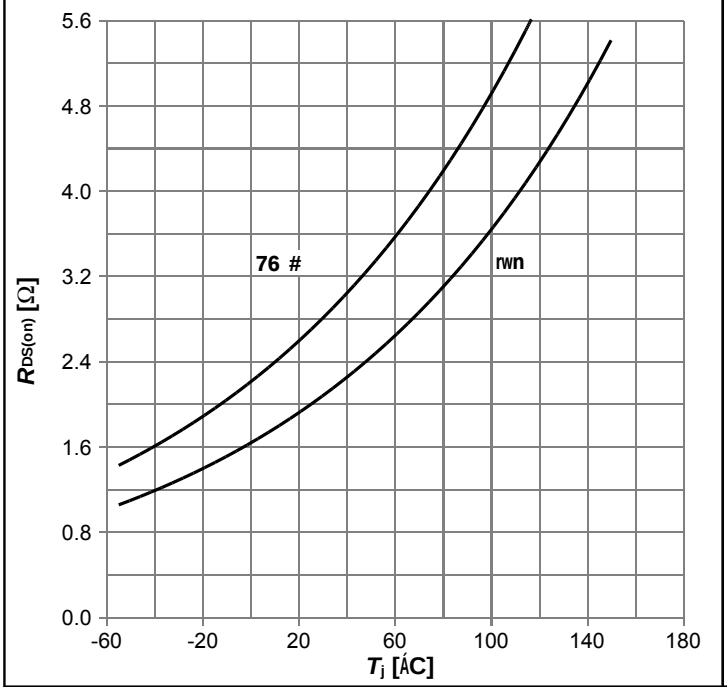
$I_D=f(V_{DS})$; T_j=150 °C; t_p=10 µs; parameter: V_{GS}

Diagram 6: Typ. drain-source on-state resistance



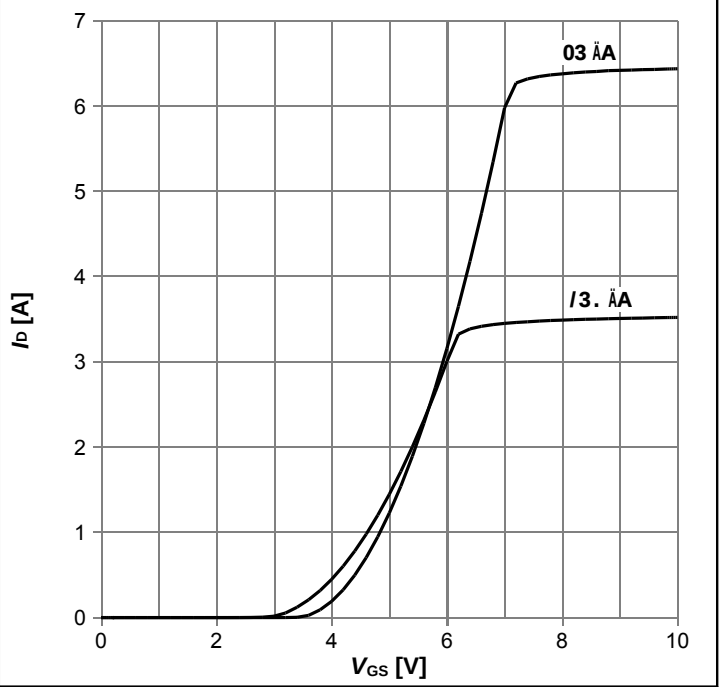
$R_{DS(on)}=f(I_D)$; T_j=150 °C; parameter: V_{GS}

Diagram 7: Drain-source on-state resistance



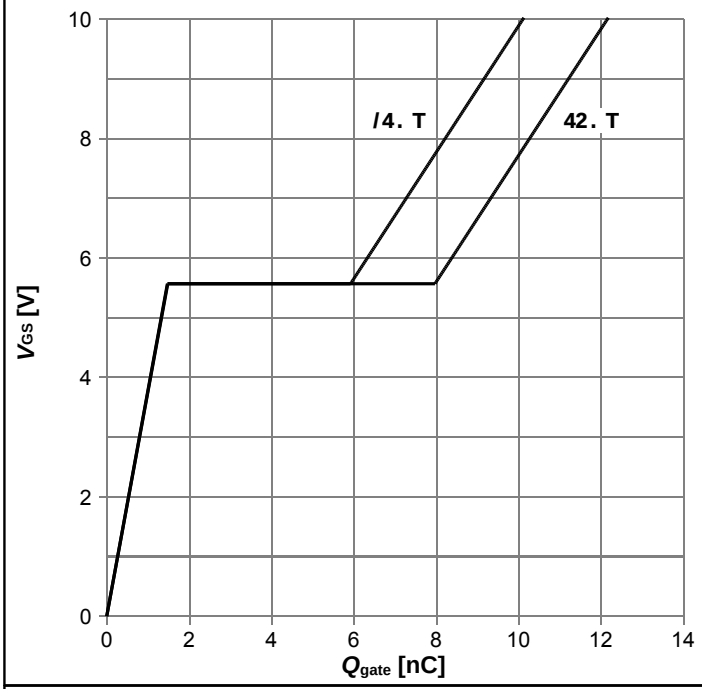
$R_{DS(on)}=f(T_j)$; I_D=1.1 A; V_{GS}=10 V

Diagram 8: Typ. transfer characteristics



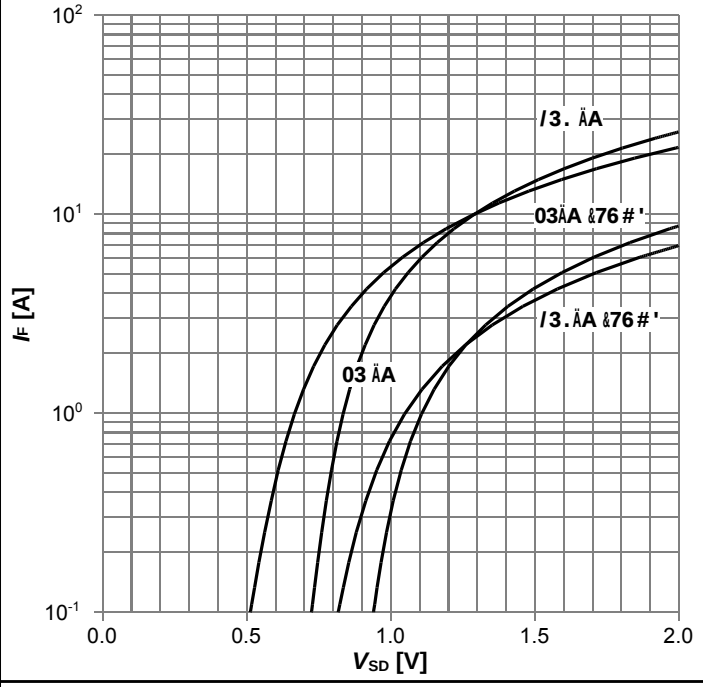
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; t_p=10 µs; parameter: T_j

Diagram 9: Typ. gate charge



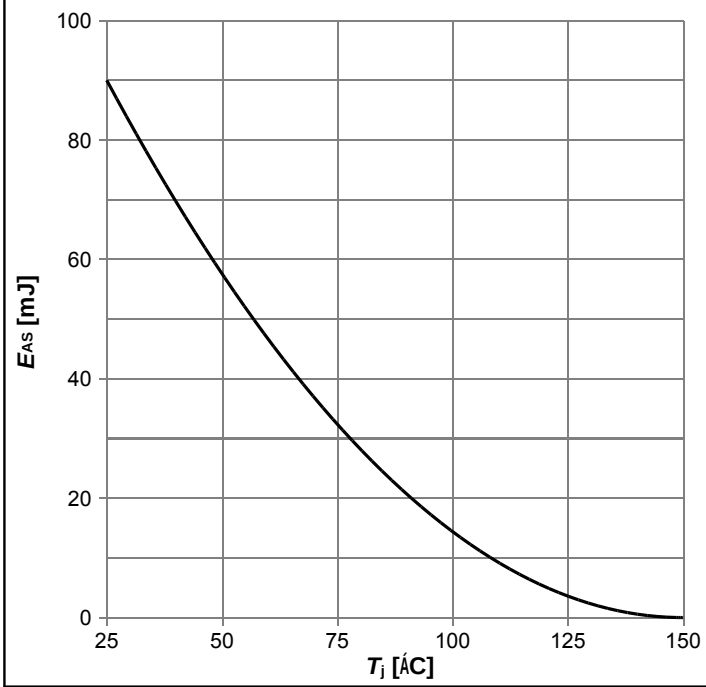
V_{GS}=f(Q_{gate}); I_D=1.9 A pulsed; parameter: V_{DD}

Diagram 10: Forward characteristics of reverse diode



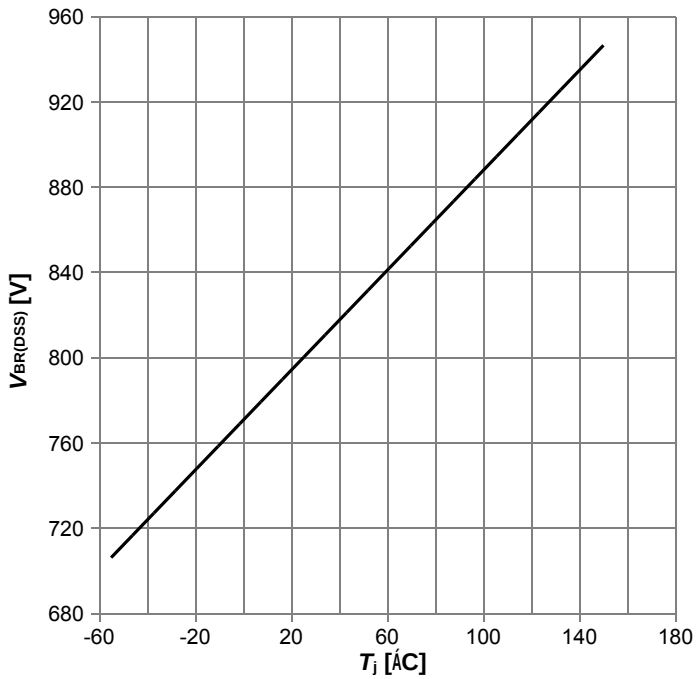
I_F=f(V_{SD}); t_p=10 µs; parameter: T_j

Diagram 11: Avalanche energy



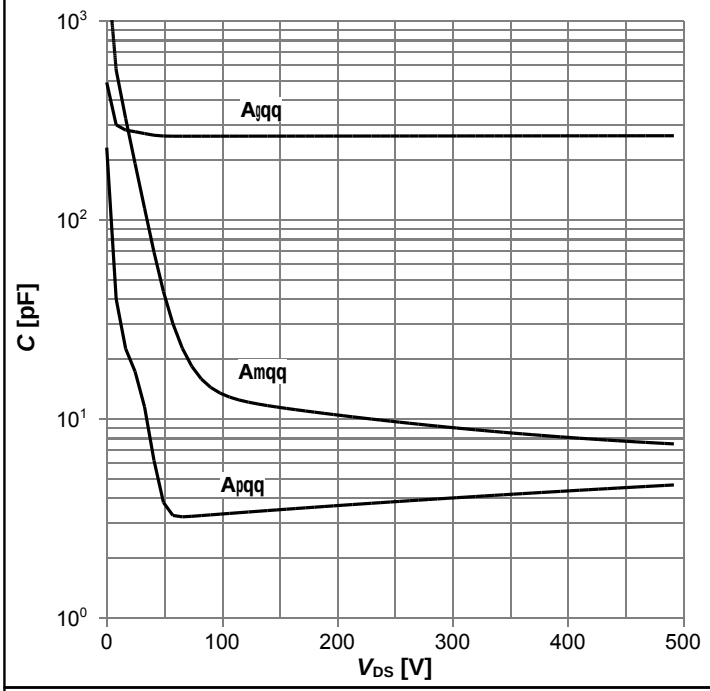
E_{AS}=f(T_j); I_D=1 A; V_{DD}=50 V

Diagram 12: Drain-source breakdown voltage



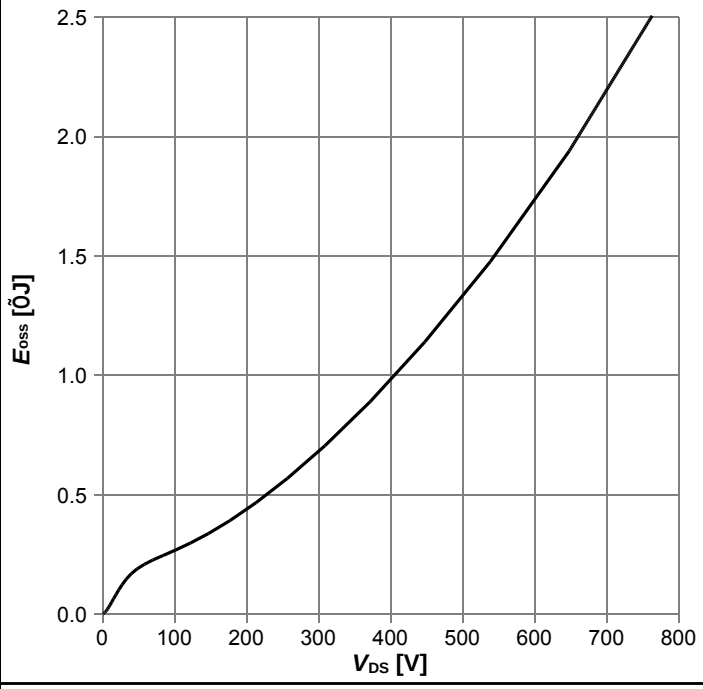
$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA

Diagram 13: Typ. capacitances



C=f(*V*$_{DS}$); *V*$_{GS}$=0 V; *f*=1 MHz

Diagram 14: Typ. Coss stored energy



E$_{oss}$=f(*V*$_{DS}$)

6 Test Circuits

Table 8 Diode characteristics

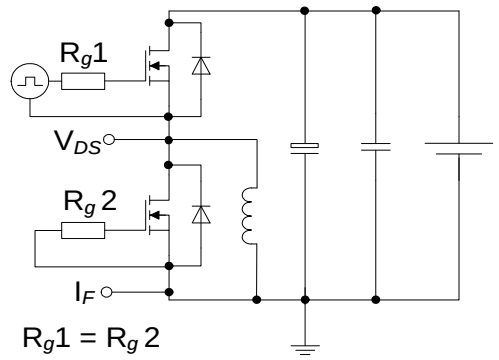
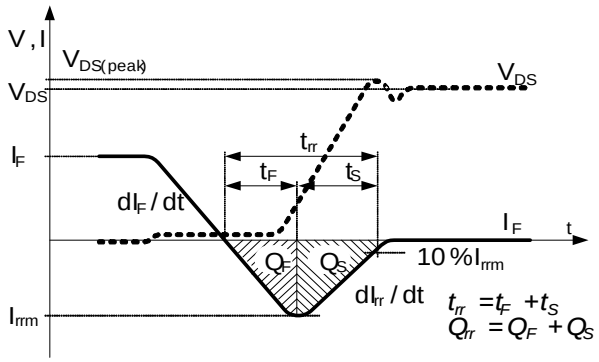
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

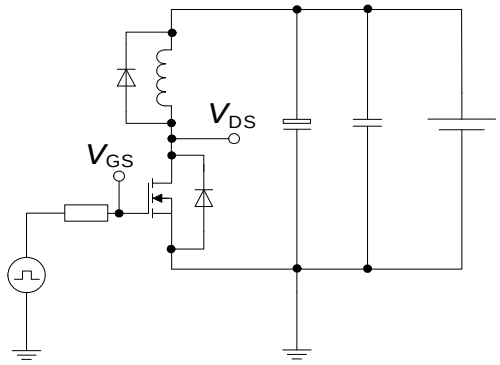
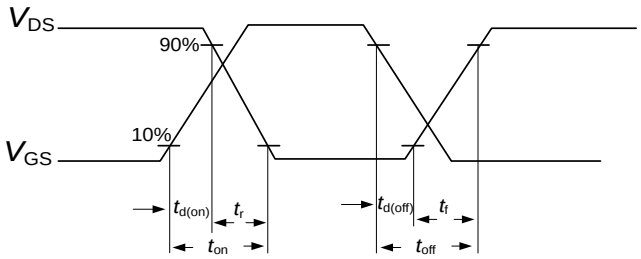
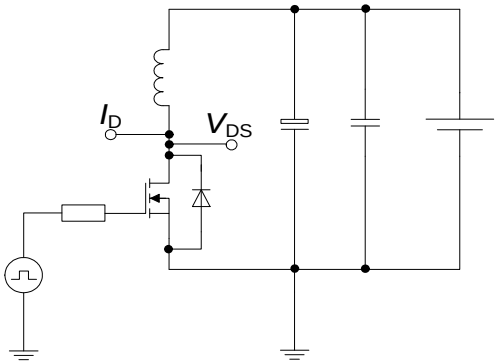
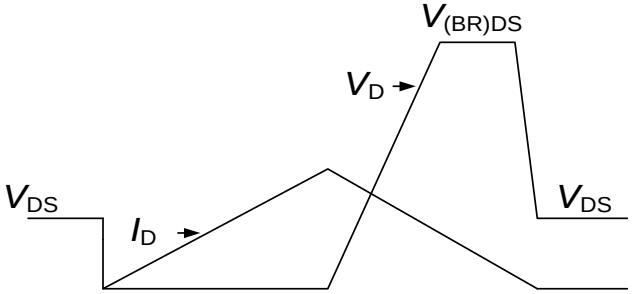
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines

Figure 1 Outline PG-TO 252, dimensions in mm/inches