# SILICON DARLINGTON POWER TRANSISTOR

Monolithic high voltage npn Darlington circuit with integrated speed-up diode in a plastic SOT93 envelope, intended for fast switching application.

## QUICK REFERENCE DATA

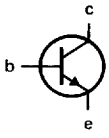
| | | | BU826 | BU826A | |
|---|---|---|---|---|---|
| Collector-emitter voltage (peak value; $V_{BE}$ = 0) | $V_{CESM}$ | max. | 800 | 900 | V |
| Collector-emitter voltage (open base) | $V_{CEO}$ | max. | 375 | 400 | V |
| Collector-emitter saturation voltage | $V_{CEsat}$ | max. | 2,0 | | V |
| Collector current (DC) | $I_C$ | max. | 6 | | A |
| Collector current (peak value) | $I_{CM}$ | max. | 8 | | A |
| Total power dissipation up to $T_{mb}$ = 25 °C | $P_{tot}$ | max. | 125 | | W |
| Collector saturation current | $I_{Csat}$ | max. | 2,5 | | A |
| Fall time | $t_f$ | typ. | 0,2 | | μs |

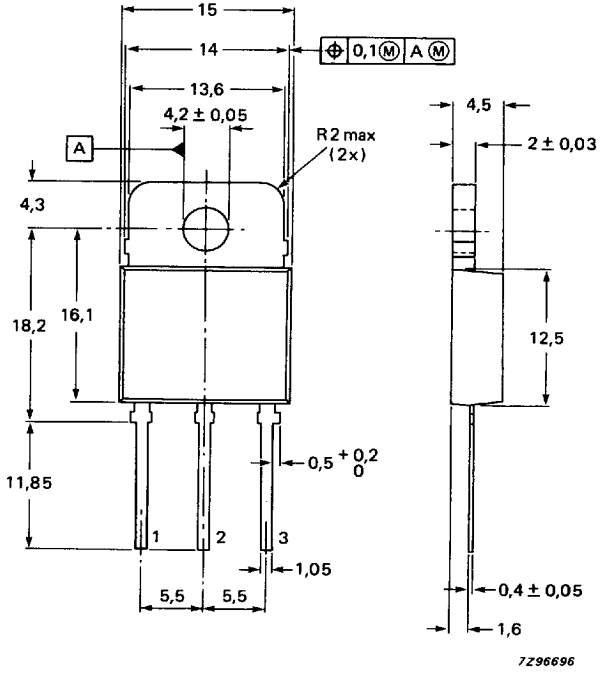
## MECHANICAL DATA

Dimensions in mm

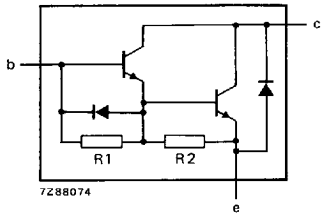
Fig. 1 SOT93.

Collector connected to mounting base.




Pinning:
1 = base
2 = collector
3 = emitter




R1 typ. 200 Ω
R2 typ. 100 Ω

Fig. 2 Circuit diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | BU826 | BU826A | |
|---|---|---|---|---|---|
| Collector-emitter voltage (peak value; $V_{BE}$ = 0) | $V_{CESM}$ | max. | 800 | 900 | V |
| Collector-emitter voltage (open base) | $V_{CEO}$ | max. | 375 | 400 | V |
| Collector current (DC) | $I_C$ | max. | 6 | | A |
| Collector current (peak value) | $I_{CM}$ | max. | 8 | | A |
| Saturation | $I_{Csat}$ | max. | 2,5 | | A |
| Base current (DC) | $I_B$ | max. | 2 | | A |
| Base current (peak value) | $I_{BM}$ | max. | 3 | | A |
| Total power dissipation up to $T_{mb}$ = 25 °C | $P_{tot}$ | max. | 125 | | W |
| Storage temperature range | $T_{stg}$ | | −65 to + 150 | | °C |
| Junction temperature* | $T_j$ | max. | 150 | | °C |

**THERMAL RESISTANCE***

| | | | | |
|---|---|---|---|---|
| From junction to mounting base | $R_{th\ j\text{-}mb}$ | = | 1,0 | K/W |

* Based on maximum average junction temperature in line with common industrial practice. The resulting higher junction temperature of the output transistor part is taken into account.

## CHARACTERISTICS

$T_j$ = 25 °C unless otherwise specified

| | | | |
|---|---|---|---|
| Collector cut-off current* | | | |
| $V_{CE} = V_{CESMmax}$; $V_{BE} = 0$ | $I_{CES}$ | max. | 1 mA |
| $V_{CE} = V_{CESMmax}$; $V_{BE} = 0$; $T_j$ = 125 °C | $I_{CES}$ | max. | 2 mA |
| Emitter cut-off current | | | |
| $I_C = 0$; $V_{EB} = 8$ V | $I_{EBO}$ | max. | 150 mA |
| | | min. | 50 mA |
| Collector-emitter sustaining voltage | | | |
| $I_C$ = 100 mA; $I_{Boff} = 0$; L = 25 mH | $V_{CEOsust}$ | min. | 375 V |
| Saturation voltages | | | |
| $I_C$ = 2,5 A; $I_B$ = 55 mA | $V_{CEsat}$ | max. | 2,0 V |
| | $V_{BEsat}$ | max. | 2,2 V |
| $I_C$ = 4 A; $I_B$ = 200 mA | $V_{CEsat}$ | max. | 2,5 V |

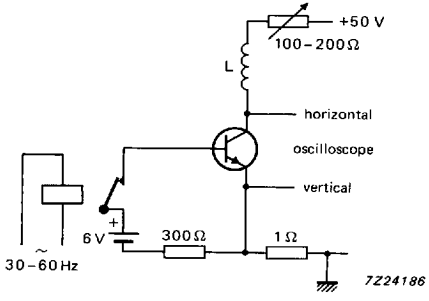



Fig. 3 Test circuit for $V_{CEOsust}$.

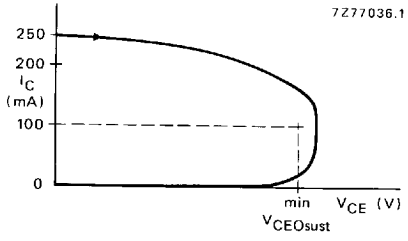



Fig. 4 Oscilloscope display for $V_{CEOsust}$.

* Measured with a half-sinewave voltage (curve tracer).

**CHARACTERISTICS** (continued)

Switching times (between 10% and 90% levels)

$I_{Con}$ = 2,5 A; $V_{CC}$ = 250 V

$I_{Bon}$ = 55 mA; $-I_{Boff}$ = 1 A

| | | | |
|---|---|---|---|
| Turn-on time | $t_{on}$ | max. | 1,3 μs |
| Turn-off time: Storage time | $t_s$ | max. | 2,0 μs |
| Fall time | $t_f$ | typ. | 0,2 μs |
| Fall time; $T_{mb}$ = 100 °C | $t_f$ | max. | 0,6 μs |

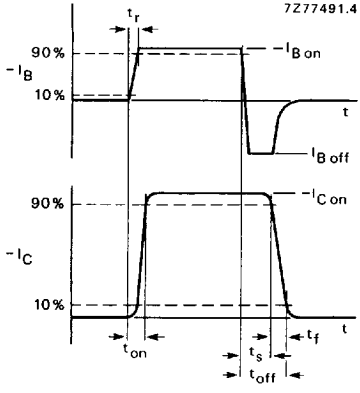



Fig. 5 Waveforms.

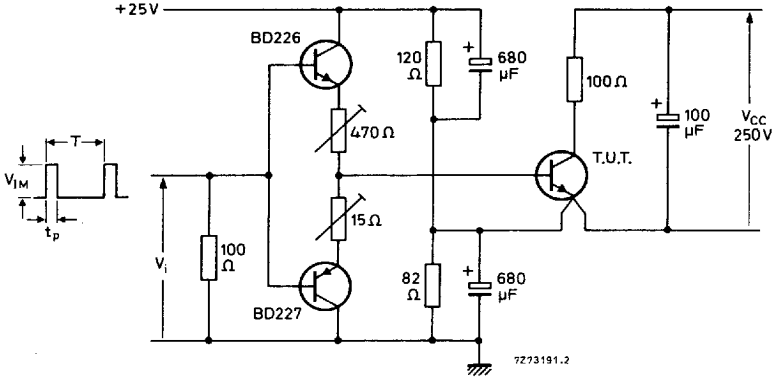
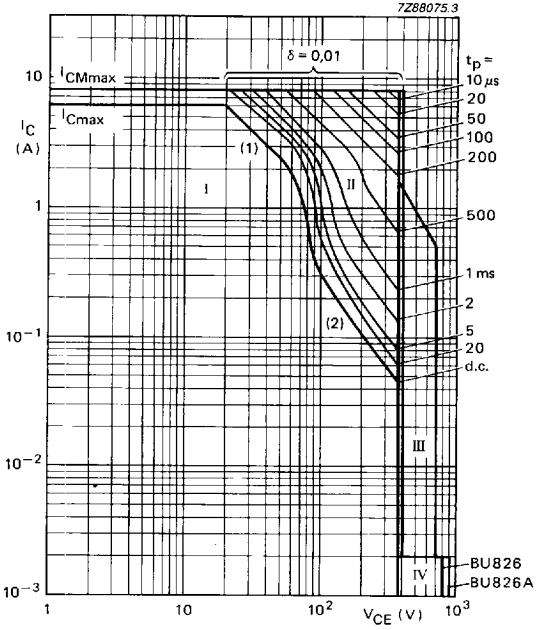



Fig. 6 Test circuit. T = 2 ms; $t_p$ = 20 μs; $V_{IM}$ = 15 V.




I Region of permissible DC operation.
II Permissible extension for repetitive pulse operation.
III Area of permissible operation during turn-on in single-transistor converters, provided $t_p < 1{,}3$ μs.
IV Repetitive pulse operation in this region is permissible, provided $V_{BE} \leqslant 0$ and $t_p \leqslant 2$ ms.

(1) $P_{tot\ max}$ and $P_{peak\ max}$ lines.
(2) Second-breakdown limits.

Fig. 7 Safe operating area at $T_{amb}$ = 25 °C.

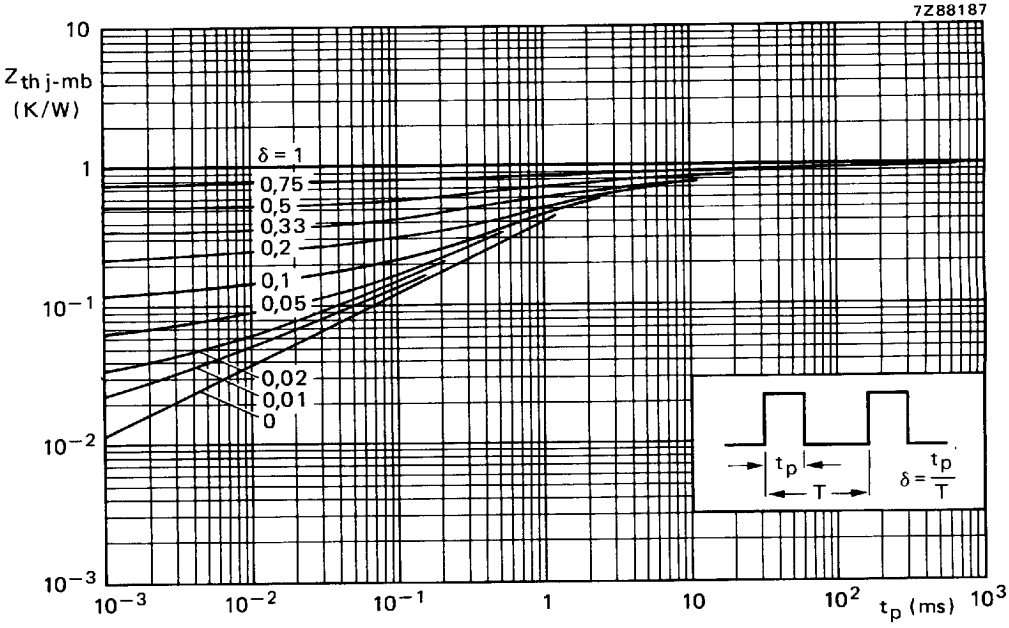



Fig. 8 Pulse power rating chart.

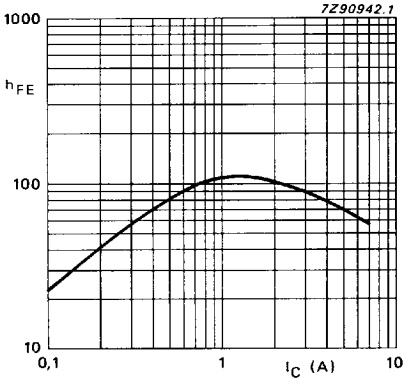



Fig. 9 DC current gain; $V_{CE}$ = 5 V; $T_j$ = 25 °C.

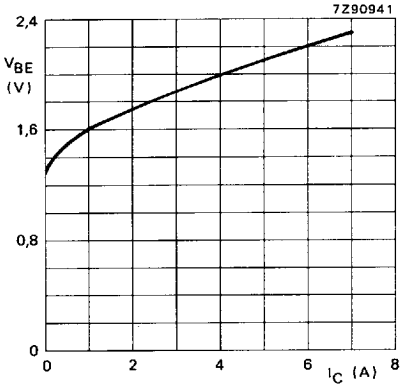



Fig. 10 $V_{BEsat}$ curve; $T_j$ = 25° C; typical values.