NPN EPITAXIAL PLANAR SILICON TRANSISTOR

CSC1815

TO-92

TO-92
Leaded Plastic
Package
RoHS compliant

(Complementary CSA1015)

APPLICATIONS: Audio Frequency General Purpose and Driver Stage Amplifier Applications.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

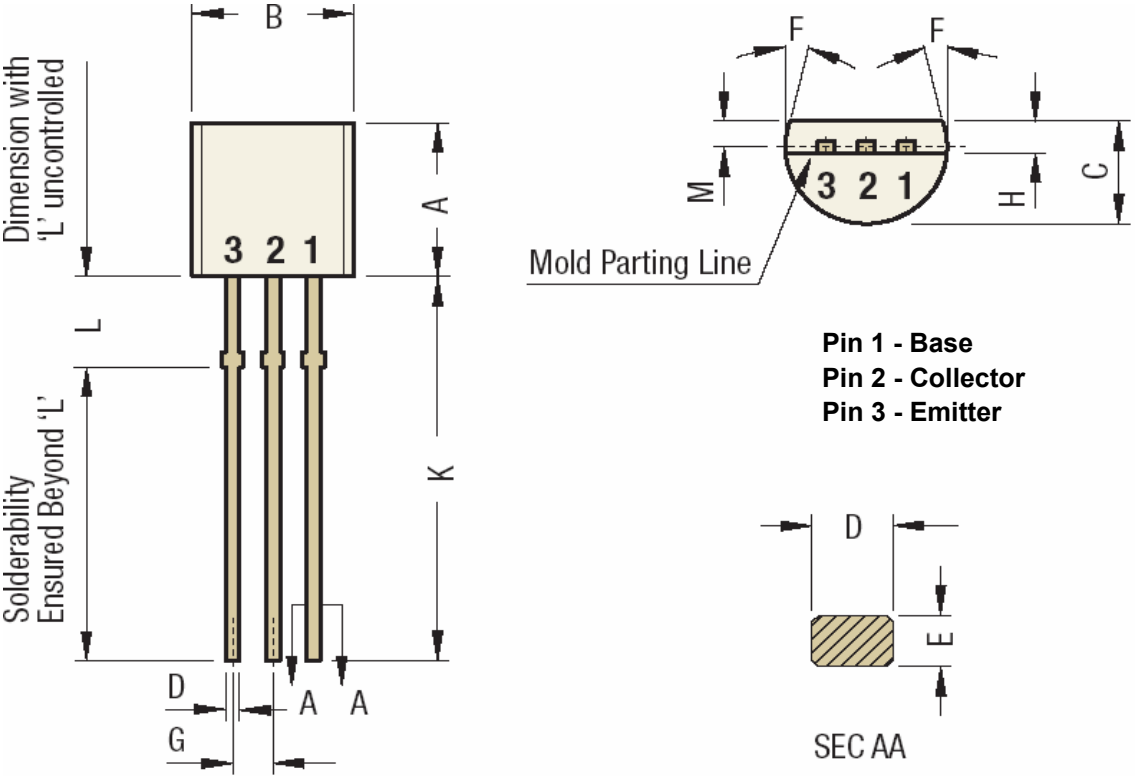
DESCRIPTION	SYMBOL	VALUE	UNITS
Collector Base Voltage	V_{CBO}	60	V
Collector Emitter Voltage	V_{CEO}	50	V
Emitter Base Voltage	V_{EBO}	5	V
Collector Current Continuous	I_C	150	mA
Base Current	I_B	50	mA
Collector Power Dissipation	P_C	625	mW
Operating And Storage Junction Temperature Range	T_j, T_{stg}	-55 to +125	ºC
THERMAL RESISTANCE			
Junction to case	$R_{\theta(j-c)}$	250	ºC/W

ELECTRICAL CHARACTERISTICS at T_a = 25 °C

DESCRIPTION	SYMBOL	TEST CONDITION	VALUE			UNITS
			MIN	TYP	MAX	
Collector Cut off Current	I_{CBO}	V_{CB} =60V, I_E=0	-	-	100	nA
Emitter Cut off Current	I_{EBO}	V_{EB}=5V, I_C = 0	-	-	100	nA
DC Current Gain	*h_{FE}	I_C =2mA, V_{CE}=6V	70	-	700	
	h_{FE}	I_C =150mA, V_{CE}=6V	25	-	-	
Collector Emitter Saturation	$V_{CE(sat)}$	I_C=100mA, I_B= 10mA	-	-	0.25	V
Base Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=100mA, I_B= 10mA	-	-	1	V
Dynamic Characteristics						
Transition Frequency	f_t	V_{CE} =10V, I_C=1mA, f =100MHz	80	-	-	MHz
Collector Output Capacitance	C_{ob}	V_{CB} =10V, I_E=0, f =1MHz	-	-	3	pF
Base Spreading Resistance	$r_{bb'}$	V_{CB}=10V, I_E=1mA, f =30MHz	-	50	-	Ω
Noise Figure	NF	V_{CE}=6V, I_C=0.1mA, R_g=10KW, f =1KHz	-	-	10	dB

CLASSIFICATION	O	Y	GR	BL
*h_{FE}	70 - 140	120 - 240	200 - 400	350 - 700

PACKAGE DETAILS

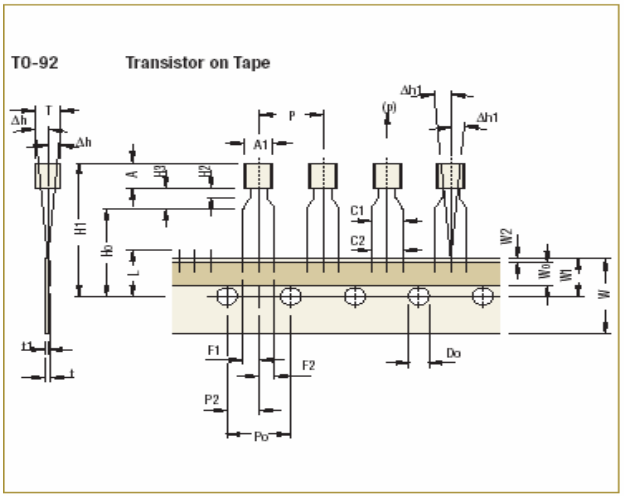


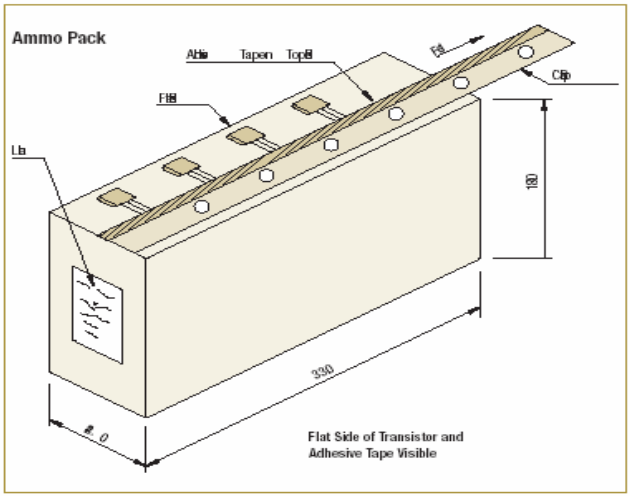
DIM	Min	Max
A	4.32	5.33
B	4.45	5.2
C	3.18	4.19
D	0.4	0.55
E	0.3	0.55
F	5º	

DIM	Min	Max
G	1.14	1.4
H	1.2	1.4
K	12.7	
L	1.98	2.082
M	1.03	1.2

(All Dimensions are in mm)

TO-92 Tape and Ammo Packaging





(All Dimensions are in mm)

Tape Specifications

		TO-92			
Item description	Symbol	Min	Nom	Max	Tol
Body width	A1	4.45		5.20	
Body height	A	4.32		5.33	
Body thickness	T	3.18		4.19	
Pitch of component[Cr]	P		12.7		±1.0
Feed hole pitch[§1]	Po		12.7		±0.3
Feed hole center to component centre[§2]	P2		6.35		±0.4
Comp. alignment, Side view[§3]	Dh		0	1.0	
Comp. alignment, Front view[§3]	Dh1		0	1.3	
Tape width[Cr]	W		18		±0.5
Hold down tape width[Cr]	Wo		6		±0.2
Hole position	W1		9		+0.7 -0.5
Hold-down tape position	W2	0.0		0.7	
Lead wire clinch height	Ho		16		±0.5
Component height	H1			24.0	
Length of snipped leads	L			11.0	
Feed hole diameter[Cr]	Do		4		±0.2
Total tape thickness[§4]	t			1.2	
Lead-to-lead distance[Cr]	F1, F2	2.4		2.7	
Stand off	H2	0.45		1.45	
Clinch height	H3			3.0	
Lead parallelismCr	C1-C2			0.22	
Pull-out force	(p)	6N			

Taping Specification

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.
§2 To be measured at bottom of clinch.
§3 At top of body.
§4 t1 = 0.3 – 0.6 mm
Cr Critical Dimension.

(All Dimensions are in mm)

Packaging Information

T & A: Tape and Ammo Pack; T & R: Tape and Red; Bulk: Loose in Poly bags; Tube: Tube and Ammo Pack; k: 1.000

Package/ Case Type	Packaging Type	Std. Packing	Inner Carton			Outer Carton		
		Qty	Qty	Size L x W x H (cm)	Gross Weight (Kg)	Qty	Size L x W x H (cm)	Gross Weight (Kg)
TO-92	Bulk	1,000	5K	19x19x8	1.1	80K	43x40x35	20
	T&A	2,000	2K	32x4.5x20	0.7	40K	43x40x35	15.2

For Lead Free Parts, Device Part # will be Prefixed with "T"

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.

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